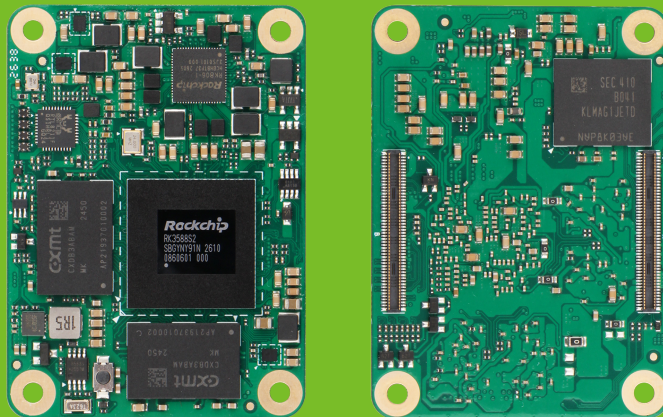

Radxa CM120

A High Performance Embedded
System-on-Module

Draft 0.8



Radxa Computer (Shenzhen) Co., Ltd.

2026-10-09

Contents

1	Revision Control Table	5
2	Introduction	6
2.1	Introduction	6
2.2	Features	7
2.3	Block Diagram	8
3	Interfaces	10
3.1	Interface Resource Overview	10
3.2	Wireless	10
3.3	Ethernet	11
3.4	PCIe	12
3.5	USB 3.1 Gen1 OTG (SuperSpeed, Type-C Electrical Interface)	13
3.6	USB 2.0 (High-Speed)	14
3.7	GPIO	14
3.8	Alternative Function Assignments	15
3.9	HDMI	15
3.10	MIPI (DSI / CSI-2)	16
3.10.1	MIPI DSI (Display, 4-lane)	16
3.10.2	MIPI CSI-2 CAM1 (4-lane)	17
3.10.3	MIPI CSI-2 CAM2 (2-lane)	17
3.11	SDIO / eMMC	18
3.12	USB-C (CC1 / CC2)	18
3.13	Fan Control	18
3.14	PMIC_EN / PWR_BUT	19
3.15	VBAT / RTC	19
3.16	Boot Mode / Recovery	19
3.17	LED	20
3.18	EEPROM_NWP / On-Board EEPROM	20
3.19	Debug UART	21
3.20	Other Low-Speed Interface Summary	21
3.21	Reset / Recovery Modes (Maskrom / Recovery)	22
3.22	Power Pins (Interface Side)	23
4	Electrical and Mechanical	24
4.1	Mechanical	24
4.1.1	Outline Dimensions	24
4.1.2	Board-to-Board Connectors and Stacking Heights	26
4.1.3	Assembly and Layout Notes	27

4.2	Thermal	28
4.2.1	Temperature Ranges	28
4.2.2	SoC Package Thermal Characteristics	28
4.2.3	Temperature Monitoring and Protection	29
4.2.4	Thermal Design Requirements	29
4.3	Electrical Specification	29
4.3.1	Absolute Maximum Ratings (Module Level)	30
4.3.2	Recommended Operating Conditions	30
4.3.3	GPIO DC Characteristics	31
4.3.4	High-Speed Interface Transmit/Receive Electrical Characteristics (PCIe 2.1 / SATA 3.0 Combo PIPE PHY)	33
4.3.5	Module-Internal Power Architecture Overview	34
4.3.6	Power Consumption	35
5	Pinout	37
5.1	Pin Definitions (Pins 1–100, First Connector)	37
5.2	Pin Definitions (Pins 101–200, Second Connector)	40
6	Power	43
6.1	Power Architecture Overview	43
6.1.1	Power Input	43
6.1.2	Power Tree	44
6.1.3	Pre-Regulator Buck (U2 JW5265 → VCC_SYSIN)	44
6.1.4	Power Management Device Summary	45
6.2	Power-up Sequencing	46
6.2.1	Power-up Preconditions	46
6.2.2	Power-on Trigger Methods	46
6.2.3	RK806-1 Power-up Sequencing (Main PMIC)	47
6.2.4	EXT_EN Auxiliary Power Chain (VCC_1V1_NLDO_S3) △	48
6.2.5	RK860 Big-Core/NPU Supplies	48
6.2.6	External Output Rails (3V3_O / 1V8_O) Power-up Order △ Opposite to CM5	49
6.2.7	Power-up Sequence Summary	49
6.3	Power-down Sequencing	50
6.3.1	Normal Shutdown Procedure	50
6.3.2	Shutdown Trigger Methods (RK806-1: 7 Methods)	50
6.3.3	Power-down Order	51
6.3.4	Reset (Non-Power-down) Behavior	52
6.3.5	+5V Loss and RTC Survival	52
6.4	Power Consumption	53
6.4.1	Module-Level Power Consumption	53

6.4.2	Power Device Quiescent/Shutdown Currents (Chip-Level Reference Values)	53
6.4.3	Form-Factor Reference (CM5 Measured Values, Not CM120 Specifications)	54
6.5	Regulator Outputs	54
6.5.1	Output Rails to the Carrier Board	54
6.5.2	Module-Internal Power Rail Summary	55
6.6	Power-Related Control and Auxiliary Circuits	57
6.6.1	PMIC_ENABLE (Pin 99 → RK806 PWRON)	57
6.6.2	PWR_BUT (Pin 92 → PMIC_RESET_L / RK806 RESETB Node)	58
6.6.3	VRTC and RTC Backup (Pin 78)	58
6.6.4	VDC Automatic Power-on Trigger Circuit (Module-Internal)	59
6.6.5	PMIC Management Signals	59
6.6.6	I2C Power Management Buses	60
6.6.7	HDMI 5V (HDMI_5V)	60
6.7	Protection Features	60
7	Appendix D: Abbreviations and Definitions	62

List of Figures

1	Radxa CM120 module	6
2	Radxa CM120 system block diagram	9
3	Radxa CM120 outline dimensions (top and bottom views)	25

List of Tables

1	Revision Control Table	5
51	Pin definitions (pins 1–100, first connector)	37
52	Pin definitions (pins 101–200, second connector)	40
67	RK806-1 BUCK Outputs (VCC_SYSIN Input)	55
68	RK806-1 NLDO Outputs (Input = VCC_1V1_NLDO_S3, via VCC13/VCC14)	55
69	RK806-1 PLDO Outputs (Input = VCC_2V0_PLDO_S3, via VCC11)	56
70	RK860 Outputs (VCC_SYSIN Input)	56
71	Pre-Regulator and Auxiliary Supplies	57
72	External Output Domains (via Connector)	57

1 Revision Control Table

Table 1: *Revision Control Table*

Version	Date	Changes from previous version
0.8	2026-10-09	First version

2 Introduction

2.1 Introduction

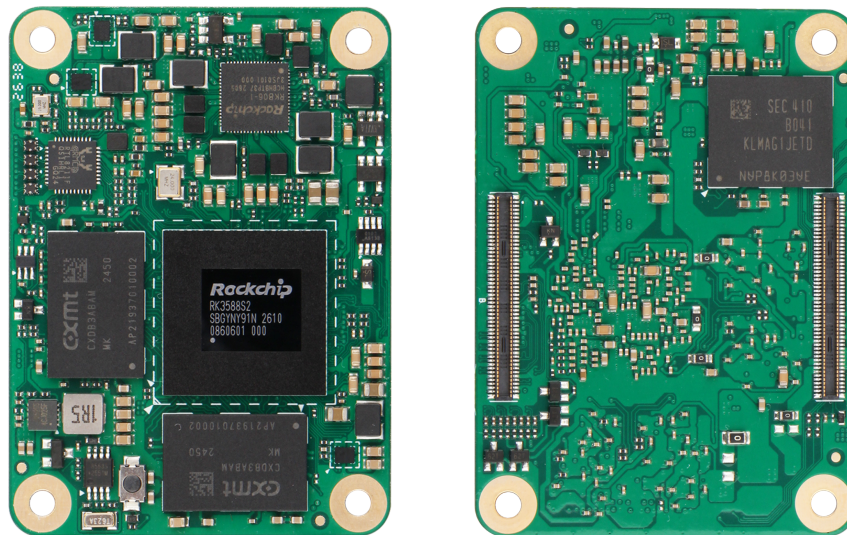


Figure 1: Radxa CM120 module

The CM120 is a System on Module (SoM) designed for deeply embedded applications. It integrates the host processor (Rockchip **RK3588S**, FCCSP1253L package, 17 mm × 17 mm), dual-channel **LPDDR4** (two BGA200 devices, 2GB/4GB/8GB/16GB capacity options), **eMMC 5.1** Flash (16GB/32GB/64GB capacity options), a Gigabit Ethernet PHY (Realtek **RTL8211F-CG**), the power management unit (Rockchip **RK806** + 3 × **RK860**), and a real-time clock (**HYM8563TS**).

The module adopts the **Raspberry Pi Compute Module 5 electrical and mechanical form factor**: all external electrical interfaces are routed out through **two 100-pin high-density board-to-board connectors** (represented as a single symbol U7 in the schematic; netlist pins 1–100 and 101–200 correspond to the two connectors respectively; the module-side connector is **Hirose DF40C-100DP-0.4V**; mating connectors and stacking heights are specified in Section 4.1.2). A carrier board (IO Board) may extend power supplies, network interfaces, memory card sockets, and various external devices on top of these interfaces.

Key differences from the Raspberry Pi CM5: the CM120 is **not equipped** with a wireless communication module; the second HDMI (HDMI1) pin group and the second USB3 (USB3-

1) pin group on the module connector are **multiplexed** as the USB3.1 Gen1 OTG (Type-C, DP Alt Mode capable) differential channels and the second PCIe 2.1 x1 lane respectively (refer to Chapter 3 and the Pinout chapter).

System boot: the RK3588S BootROM supports booting from eMMC and SD/MMC, as well as code download via USB OTG (per RK3588S Datasheet Section 1.2.2). Boot mode selection is implemented through voltage sampling (SARADC_IN0_BOOT) of the connector **NRPIBOOT** pin and the on-module recovery pushbutton **SW1** (refer to Section 3.16).

2.2 Features

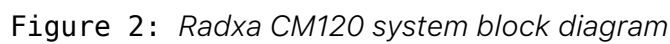
The key features of the CM120 are listed below (SoC capability items per RK3588S Datasheet V1.4; the module implementation scope is defined by the netlist):

Category	Feature
Processor	Rockchip RK3588S: 4 × ARM Cortex-A76 + 4 × ARM Cortex-A55 (big.LITTLE), 3 MB shared L3 cache; operating frequency TBD
Graphics Processor (GPU)	ARM Mali-G610 MP4; compatible with OpenGL ES 1.1/2.0/3.2, OpenCL 2.2, Vulkan 1.2
Neural Processing Unit (NPU)	Up to 6 TOPS; supports INT4/INT8/INT16/FP16/BFloat16/TF32; three cores operable cooperatively or independently
Video Codec (VPU)	Decoding: H.265/VP9/AVS2 8K@60fps, H.264 8K@30fps, AV1 4K@60fps; encoding: H.264/H.265 up to 8K@30fps; JPEG codec (encoding 8192×8192, four encoding units)
Image Signal Processor (ISP)	Up to 48 MP; supports 3A, HDR, 3DNR, LSC and other processing (multi-sensor multiplexing)
Memory	2 × LPDDR4 (BGA200, 2GB/4GB/8GB/16GB capacity options), interfaced to the RK3588S DDR controller (SoC supports LPDDR4/LPDDR4X/LPDDR5, four channels, 16-bit per channel)
Storage	On-board eMMC 5.1: KLM8G1GETF-B041, 16GB/32GB/64GB capacity options, supports HS400/HS200/DDR50/legacy modes, 8-bit bus
Ethernet	1 × 10/100/1000 Mbps, RK3588S GMAC (RGMII) + RTL8211F-CG PHY; MDI differential pairs routed directly to the connector
USB	1 × USB 3.1 Gen1 OTG (5 Gbps, Type-C electrical interface, DP Alt Mode capable); 1 × USB 2.0 OTG (High-Speed); 1 × USB 2.0 Host (High-Speed)
PCIe	2 × PCIe 2.1 x1 (5 Gbps per lane, RC mode only); Channel A on the connector PCIe pin group, Channel B multiplexed on the USB3-1 pin group
Display	1 × HDMI TX0 (FRL rates 3/6/8/10/12 Gbps, SoC rated up to 7680×4320@60 Hz; HDCP 2.3) — routed via 4 AC-coupled data lanes + DDC/HPD/CEC; 1 × MIPI DSI (4-lane, up to 4.5 Gbps per lane, up to 4K@60 Hz)
Camera Inputs	2 × MIPI CSI-2: CAM1 (4-lane, MIPI DPHY V1.2, 2.5 Gbps per lane); CAM2 (2-lane); each with dedicated I2C and control signals

Category	Feature
Low-Speed Interfaces	GPIO (26 connector GPIO bits), I2S1 (8-channel), SPI4, UART2 (debug), UART5/CAN2, I2C (I2C5/I2C6/I2C7 to connector), PWM14, SDIO (SDMMC0, 4-bit)
Real-Time Clock	HYM8563TS + 32.768 kHz crystal; RTC backup power supplied by the carrier board via the GPIO_VREF pin (refer to Section 3.15)
EEPROM	BL24C16F (16 Kbit, I2C0 bus); write protection controlled by SoC GPIO1_A7 via transistor Q2
Power	Single +5 V input (six paralleled 5V_IN pins); RK806 PMIC (SPI configuration bus) + 3 × RK860 (VDD_CPU_BIG0/BIG1/VDD_NPU) + JW5265 pre-regulator buck + SY8089/SQM2590 auxiliary supplies; 3.3 V (3V3_O) and 1.8 V (1V8_O) rails provided to the carrier board
Mechanical Form Factor	Raspberry Pi CM5 form factor: dual 100-pin board-to-board connectors (Hirose DF40C-100DP-0.4V); PCB outline 55.0 mm × 40.0 mm ; mounting holes 4 × φ2.7 mm (hole centers 3.5 mm from board edges); module thickness / PCB thickness TBD (CM5 form factor reference: 4.6 mm / 1.24 mm ±10%)
Wireless	No WiFi/BT module populated; connector WL_nDISABLE / BT_nDISABLE pins are multiplexed as CAM2 control signals (refer to Section 3.2)

2.3 Block Diagram

The figure below shows the major functional areas of Radxa CM120.



3 Interfaces

3.1 Interface Resource Overview

Interface	SoC Resource	Connector Pins	Remarks
Gigabit Ethernet	GMAC (RGMII) + RTL8211F-CG	3–17	4 MDI pairs + 2 LEDs
USB 2.0 Host 0	USB20_HOST0	16 / 18	Pins multiplexed from FAN_TACHO / ETHERNET_SYNC_OUT
USB 2.0 OTG (Type-C data)	TYPECO_USB20_OTG	103 / 105, 101 (ID)	Shares port with USB3OTG_0
USB 3.1 Gen1 OTG (SuperSpeed)	USB3OTG_0 (Combo PHY, multiplexed with DP TX0)	146/148, 152/154, 158/160, 104/106, 164/166	Pins multiplexed from HDMI1 pin group
PCIe 2.1 ×1 (Channel A)	PCIE20_0 (Combo PHY0, multiplexed with SATA3.0)	110/112, 116/118, 122/124, 102, 109, 111	Standard PCIe pin group
PCIe 2.1 ×1 (Channel B)	PCIE20_2 (Combo PHY2, multiplexed with SATA3.0/USB3.1)	157/159, 163/165, 169/171	Pins multiplexed from USB3-1 pin group
HDMI (HDMI0)	HDMI_TX0 (multiplexed with eDP TX0)	151, 153, 170–172, 176–178, 182–184, 188–190, 199, 200	4 data pairs + DDC/HPD/CEC
MIPI DSI	MIPI_DPHY1_TX (DSI)	175–196	4 data lanes + clock pair
MIPI CSI CAM1 (4-lane)	MIPI_DPHY0_RX	115–141	+ I2C7, RST/PDN/CLKOUT (80/82/97/55/51)
MIPI CSI CAM2 (2-lane)	MIPI_CSI0 (RX)	128/130, 134/136, 140/142	+ I2C5, RST/CLKOUT/PDN (35/36/89/91/143)
SDIO (SD card)	SDMMC0 (4-bit)	57–76	Including power enable and card detect
GPIO / I2S / SPI / UART / CAN / I2C / PWM	GPIO0–GPIO4 multiplexed	19–58, etc.	Refer to Sections 3.7 / 3.8 / 3.20
Debug UART	UART2_M0	54 / 56	Refer to Section 3.19
Boot mode / recovery	SARADC_IN0_BOOT / IN1	93, on-module SW1	Refer to Section 3.16
Power input	—	77–87 (5V_IN)	Refer to Chapter 6
Power output	Generated by RK806/SQM2590	84 / 86 (3V3_O), 88 / 90 (1V8_O)	Module-to-carrier power rails
RTC backup power	—	78 (GPIO_VREF)	Refer to Section 3.15
Control signals	RK806 / GPIO	92 (PWR_BUT), 99 (PMIC_ENABLE), 20 (EEPROM_NWP), 21/95 (LED)	Refer to Sections 3.14 / 3.17 / 3.18

Note: Connector pin numbers are the netlist pin numbers of schematic symbol U7 (1–100 for the first connector, 101–200 for the second). The pin-by-pin correspondence with the Raspberry Pi CM5 form factor pinout is provided in Chapter [5](#) “Pinout”.

3.2 Wireless

The CM120 is **not equipped** with a WiFi/Bluetooth module. The wireless control pins reserved in the Raspberry Pi CM5 form factor are multiplexed as follows:

Connector Pin	Pin Name	Net Name	SoC Ball / Multiplexed Function	Direction	Remarks
89	WL_NDISABLE	MIPI_DPHY_CSI_CAM2_RST_3V3	GPIO1_B3	Output	Multiplexed as CAM2 reset (3.3 V)
91	BT_NDISABLE	MIPI_CSI_CAM2_CLKOUT_3V3	— (output via R26 network)	Output	Multiplexed as CAM2 clock output (3.3 V)

3.3 Ethernet

The RK3588S on-chip GMAC (10/100/1000 Mbps, RGMII/RMII, full/half duplex) interfaces via RGMII to an external Realtek **RTL8211F-CG** Gigabit PHY. The MDI differential pairs are routed directly to the connector through the network transformer/common-mode chokes (L2–L5).

RGMII signals (SoC ↔ PHY):

SoC Ball (Multiplexed Name)	Net	PHY Pin	Remarks
GPIO3_A7_u (GMAC1_RXD0)	GMAC1_RXD0	RXD0	RGMII receive data 0
GPIO3_B0_u	GMAC1_RXD1	RXD1	RGMII receive data 1
GPIO3_A2_u	GMAC1_RXD2	RXD2	RGMII receive data 2
GPIO3_A3_u	GMAC1_RXD3	RXD3	RGMII receive data 3
GPIO3_B1_d	GMAC1_RXDV_CRS	RXCTL	RGMII receive control
GPIO3_A5_d	GMAC1_RXCLK	RXC	RGMII receive clock
GPIO3_B3_u	GMAC1_TXD0	TXD0	RGMII transmit data 0
GPIO3_B4_u	GMAC1_TXD1	TXD1	RGMII transmit data 1
GPIO3_A0_u	GMAC1_TXD2	TXD2	RGMII transmit data 2
GPIO3_A1_u	GMAC1_TXD3	TXD3	RGMII transmit data 3
GPIO3_B5_u	GMAC1_TXEN	TXCTL	RGMII transmit control
GPIO3_A4_d	GMAC1_TXCLK	TXC	RGMII transmit clock
GPIO3_C2_d	GMAC1_MDC	MDC	MIIM clock
GPIO3_C3_d	GMAC1_MDIO	MDIO	MIIM data
GPIO3_B2_d	GMAC1_RSTN	PHYRSTB (via R66)	PHY reset (active low)
GPIO3_C1_d	GMAC1_INT_PMEB	INTB/PMEB	PHY interrupt / PME (active low)

PHY clock and configuration: The PHY uses a 25 MHz crystal Y2 (XTAL_IN/XTAL_OUT); SoC GPIO3_A6 (ETH1_REFCLKO_25M) is connected to the same node via R69 as an optional 25 MHz clock source. The PHY address (PHYAD0/1/2) and LED modes (CFG_EXT/LDO0/LDO1) are configured by resistor pull-up/pull-down (R51–R62); **refer to the schematic for specific configuration values.**

Connector pins (MDI and LED):

Connector Pin	Pin Name	Net	Remarks
3 / 5	ETHERNRT_PAIR3_P/N	PHY1_MDI3±	MDI pair 3
4 / 6	ETHERNET_PAIR1_P/N	PHY1_MDI1±	MDI pair 1
9 / 11	ETHERNRT_PAIR2_P/N	PHY1_MDI2±	MDI pair 2
10 / 12	ETHERNET_PAIR0_P/N	PHY1_MDI0±	MDI pair 0
15	ETHERNRT_NLED3(3.3V)	PHY_YLED-	PHY yellow LED (cathode, 3.3 V drive)
17	ETHERNRT_NLED2(3.3V)	PHY_GLED+	PHY green LED (anode, 3.3 V drive)

The PHY internal LDO output (REG_OUT) is filtered by L6 for internal use (PHY_REG_OUT). The PHY supply rails AVDD10/DVDD10/AVDD33/DVDD33 are generated by the module-internal power supplies (refer to Chapter 6).

3.4 PCIe

The RK3588S provides two Combo PIPE PHYs (PHY0: PCIe2.1/SATA3.0; PHY2: PCIe2.1/SATA3.0/USB3.1), each supporting 1 lane at 5 Gbps, RC (Root Complex) mode only. The CM120 configures both as **PCIe 2.1 x1**:

Channel A (PCIE20_0) — connector standard PCIe pin group:

Connector Pin	Pin Name	Net (SoC Ball)	Direction	Remarks
110 / 112	PCIE_CLK_P/N	PCIE20_0_REFCLKP/N (L42/K41)	Output	Reference clock output (frequency TBD , to be confirmed per RK3588S Hardware Design Guide)
116 / 118	PCIE_RX_P/N	PCIE20_0_RXP/N (J42/J41)	Input	Receive differential pair
122 / 124	PCIE_TX_P/N	PCIE20_0_TXP/N (H42/H41)	Output	Transmit differential pair
109	PCIE_Nrst	PCIE20X1_2_PERSTN_M0 (GPIO3_D1)	Output	Reset (active low, via SoC GPIO)
102	PCIE_CLK_NREQ	PCIE20X1_2_CLKREQN_M0 (GPIO3_C7)	Output	CLKREQ# (via SoC GPIO)
111	VBUS_EN	PCIE20X1_2_WAKEN_M0 (GPIO3_D0)	Output	WAKE# (via SoC GPIO)

Channel B (PCIE20_2) — multiplexed on connector USB3-1 pin group:

Connector Pin	Pin Name	Net (SoC Ball)	Direction	Remarks
157 / 159	USB3-1-RX_P/N	PCIE20_2_REFCLKP/N (F41/F42)	Output	Reference clock output
163 / 165	USB3-1-D_P/N	PCIE20_2_RXP/N (D42/C42)	Input	Receive differential pair
169 / 171	USB3-1-TX_P/N	PCIE20_2_TXP/N (E41/D41)	Output	Transmit differential pair

Notes:

1. The PERST#/CLKREQ#/WAKE# control signals of Channel B are not individually routed to the connector; they shall be multiplexed with the Channel A control pins or managed by the carrier board (design convention **TBD**, refer to schematic and software configuration).
2. Once PCIE20_2 is configured as PCIe, the SoC's second USB3.1 Host

(USB3OTG_2, multiplexed with this PHY) becomes unavailable.

3. Differential impedance and trace-length requirements for both lanes shall follow the schematic constraints (**TBD**).

3.5 USB 3.1 Gen1 OTG (SuperSpeed, Type-C Electrical Interface)

The SoC USB3OTG_0 (USB 3.1 Gen1, 5 Gbps, DRD dual-role) has its SuperSpeed differential channels routed out via the connector HDMI1 pin group, and supports **USB Type-C / DP Alt Mode** (DP TX 1.4a, SoC rated up to 7680×4320@30 Hz; the SSRX/SSTX balls are multiplexed with DP0_TX0–TX3 lanes).

Connector Pin	Pin Name	Net (SoC Ball)	Direction	Remarks
158 / 160	HDIM1_TX0_P/N	SSRX1P/D0P, SSRX1N/D0N (BB10/BA10)	Input	USB3 SuperSpeed RX (also DP lane 0)
152 / 154	HDIM1_TX1_P/N	SSTX1P/D1P, SSTX1N/D1N (BB11/BA11)	Output	USB3 SuperSpeed TX (also DP lane 1)
146 / 148	HDIM1_TX2_P/N	SSRX2P/D2P, SSRX2N/D2N (BB13/BA13)	Bidirectional	DP lane 2 (used in DP Alt Mode 4-lane)
104 / 106	PCIE_NWAKE / PCIE_PWR_EN	SSTX2P/D3P, SSTX2N/D3N (BB14/BA14)	Bidirectional	DP lane 3 (used in DP Alt Mode 4-lane)
164 / 166	HDIM1_CLK_P/N	TYPEC_AUXP / TYPEC_AUXN	Bidirectional	Type-C AUX1/AUX2 (via R9/R10 to SoC GPIO3_B7/GPIO3_C0)
145 / 147	HDMI1_SDA / S1_SCL	NC / N21738933	—	HDMI1 DDC pins not used as DDC in this design (reserved/unconnected; refer to schematic)
149	HDMI1_CEC	N22579586	—	Same as above
143	HDMI1_HOTPLUG	MIPI_DPHY_CSI_CAM2_PDN_3V3	Output	Multiplexed as CAM2 Power-Down control

USB 2.0 data and associated signals:

Connector Pin	Pin Name	Net	Remarks
103 / 105	USB2_N / USB2_P	USB20_OTG_DM / DP	OTG High-Speed data pair
101	USB_OTG_ID	USB20_OTG_ID (via R5)	OTG ID detection
45	GPIO24	OTG0_PWREN_H (GPIO3_D5)	OTG port power enable output
—	—	TYPEC0_USB20_VBUSDET	VBUS detect input (pulled up to VCCA_3V3_S0 via R9243; VBUS detect source provided by carrier board)
58	GPIO2	USBCC_INT_L (GPIO4_A4)	Carrier-side USB-C controller interrupt input (active low)
100	CAM_GPIO1	USB_HUB_RST_3V3 (GPIO4_B0)	Carrier-side USB Hub reset output (3.3 V)

Note: Since the HDMI1 pin group is occupied by this interface, **the module provides only one HDMI output (HDMI0, see Section 3.9)**. If DP Alt Mode is required on the carrier board, the above differential pairs shall be connected to the Type-C connector per the USB Type-C Alt Mode pin definition (SSTX1/SSRX1→TX1/RX1, DP lanes 2/3→SSTX2/SSRX2 positions, AUX→SBU); the exact mapping is determined by the carrier board design.

3.6 USB 2.0 (High-Speed)

Channel	SoC Resource	Connector Pins	Signals	Remarks
Host 0	USB20_HOST0	16 (FAN_TACHO) / 18 (ETHERNET_SYNC_OUT)	USB20_HOST0_DP / DM	Pin multiplexing note: the CM5 form factor FAN_TACHO and ETHERNET_SYNC_OUT pins are used as the USB 2.0 Host data pair in this design
OTG (USB2 portion)	TYPECO_USB20_OTG	103 / 105	USB20_OTG_DP / DM	Shares the port with USB3OTG_0 described in Section 3.5 (USB2 data pair)

Data rates: High-Speed 480 Mbps / Full-Speed 12 Mbps / Low-Speed 1.5 Mbps (per RK3588S Datasheet). **Note:** With the FAN_TACHO pin occupied, the fan tachometer function is unavailable (see Section 3.13).

3.7 GPIO

The connector provides **26 GPIO bits** (GPIO2–GPIO27 in CM5 form factor numbering), all mapped to RK3588S GPIO0–GPIO4 multiplexed pins. The default function assignment of each GPIO is listed in the table below (**the default net names represent the module's factory device-tree configuration convention; the final configuration is subject to software**):

Connector Pin	GPIO No.	SoC Ball (Multiplexed Name)	Direction	Level
58	GPIO2	GPIO4_A4_d	Bidirectional	3.3 V
56	GPIO3	GPIO0_A3_u	Bidirectional	3.3 V
54	GPIO4	GPIO0_A6_z	Bidirectional	3.3 V
34	GPIO5	GPIO4_B1_u	Bidirectional	3.3 V
30	GPIO6	GPIO4_A5_d	Bidirectional	3.3 V
37	GPIO7	GPIO1_A4_d	Bidirectional	3.3 V
39	GPIO8	GPIO1_B0_u	Bidirectional	3.3 V
40	GPIO9	GPIO3_C4_u	Bidirectional	3.3 V
44	GPIO10	GPIO0_D0_d	Bidirectional	3.3 V
38	GPIO11	GPIO3_C5_u	Bidirectional	3.3 V
31	GPIO12	GPIO1_A3_d	Bidirectional	3.3 V
28	GPIO13	GPIO4_A2_d	Bidirectional	3.3 V
55	GPIO14	GPIO1_A6_d	Bidirectional	3.3 V
51	GPIO15	via U6 level shifter	Bidirectional	3.3 V
29	GPIO16	GPIO1_A0_d	Bidirectional	3.3 V
50	GPIO17	GPIO1_B4_u	Bidirectional	3.3 V
49	GPIO18	GPIO4_B2_u	Bidirectional	3.3 V
26	GPIO19	GPIO4_A1_d	Bidirectional	3.3 V
27	GPIO20	GPIO1_A1_d	Bidirectional	3.3 V
25	GPIO21	GPIO1_A2_d	Bidirectional	3.3 V
46	GPIO22	GPIO0_C7_d	Bidirectional	3.3 V
47	GPIO23	GPIO3_D4_d	Bidirectional	3.3 V
45	GPIO24	GPIO3_D5_d	Bidirectional	3.3 V
41	GPIO25	GPIO1_B1_d	Bidirectional	3.3 V
24	GPIO26	GPIO4_A0_d	Bidirectional	3.3 V
48	GPIO27	GPIO1_B5_u	Bidirectional	3.3 V

- The SoC ball name suffixes **_u/_d/_z** are RK3588S voltage domain markers; the supply rails of each GPIO bank (VCC_1V8_S0 / VCC_3V3_S0) are specified in Chapters 4/6. The IO level of each individual pin **shall be subject to the final schematic annotation (TBD)**.
- The CM5 form factor GPIO0, GPIO1, and GPIO28 bits are not used in the CM120 netlist (**TBD**: left floating or tied to a fixed level; refer to schematic).
- Interrupt, pull-up/pull-down, and drive strength of all GPIOs are configurable within the SoC (per RK3588S Datasheet Section 1.2.14).

3.8 Alternative Function Assignments

RK3588S GPIOs support multiple multiplexing modes M0–M3 (the net name suffix **_M0/_M1/_M2** indicates the currently selected mode). The current mode is annotated in the “default function” column of the table above; for the complete multiplexing matrix refer to “Rockchip RK3588S PinOut V10” (accompanying document) and RK3588S Datasheet Chapter 2. Multiplexing groups used on this module:

SoC Multiplex Group (Net Name)	Current Mode	Connector GPIO Bits
UART2_M0 (debug UART)	M0	GPIO3 / GPIO4
UART5_M1 / CAN2_M0	UART5=M1 / CAN2=M0	GPIO9 / GPIO11
SPI4_M2	M2	GPIO12 / GPIO16 / GPIO20 / GPIO21
I2C6_M0 (touch panel)	M0	GPIO10 / GPIO22
I2C5_M2 (CAM2)	M2	ID_SD (36) / ID_SC (35)
I2C7_M2 (CAM1)	M2	SDA0 (82) / SCL0 (80)
I2S1_M0	M0	GPIO5 / GPIO6 / GPIO13 / GPIO18 / GPIO19 / GPIO26
PWM3_IR_M3 (EEPROM_NWP)	M3	Pin 20
PWM14_M0 / CAM3_CLK_M0	M0	FAN_PWM (19)

3.9 HDMI

The CM120 routes out **one HDMI transmit channel (HDMI_TX0)**, mapped to the connector HDMI0 pin group. On the RK3588S, HDMI_TX0 shares physical pins with eDP TX0 (the module selects the HDMI function), supporting HDMI FRL rates of 3/6/8/10/12 Gbps, RGB/YUV (up to 10-bit), DSC 1.2a, and HDCP 2.3 (per RK3588S Datasheet).

TMDS/FRL differential pairs (routed via AC coupling capacitors C90593–C90600):

Connector Pin	Pin Name	SoC Ball (HDMI_TX0_Dx/EDP_TX0_Dx)	Remarks
182 / 184	HDIM0_TX0_P/N	D0P/D0N (BB4/BA4)	Data lane 0
176 / 178	HDIM0_TX1_P/N	D1P/D1N (BA5/BB5)	Data lane 1
170 / 172	HDIM0_TX2_P/N	D2P/D2N (BB7/BA7)	Data lane 2
188 / 190	HDIM0_CLK_P/N	D3P/D3N (BA2/BB2)	Data lane 3 (multiplexed onto CLK pin position)
—	—	HDMI_TX0_SBDP/SBDN (BA1/AY1)	SBDS/AUX pair not routed; AC-terminated to ground via C1/C2

Auxiliary signals:

Connector Pin	Pin Name	Net	Circuit	Remarks
199 / 200	HDIM0_SDA / SCL	HDMI_TX0_SDA_5V / SCL_5V	RS0102YH8 (U4) bidirectional level shifter (3.3 V ↔ 5 V)	DDC bus; module side connects via U4 to SoC GPIO4_C0 / GPIO4_B7 (HDMI_TX0_SDA_M0 / SCL_M0)
153	HDMI0_HOTPLUG	HDMI_TX0_HPD_PORT	R95608/R95610 divider + C3	HPD hot-plug detect input (to SoC GPIO1_A5, HDMI_TX0_HPD_M0)
151	HDMI0_CEC	HDMI_TX0_CEC_PORT	Q5013 (2SK3018) level shifter, gate tied to HMDI_5V	CEC bus (SoC side GPIO4_C1, HDMI_TX0_CEC_M0)
—	—	HDMI0_TX_ON_H (GPIO4_B6)	FB1	HDMI transmit enable control (TBD: controlled target per schematic)
—	—	HMDI_5V	D5 (B5819WS Schottky) + C26	DDC level reference supply (≈5 V, generated on module; source rail per schematic)

3.10 MIPI (DSI / CSI-2)

3.10.1 MIPI DSI (Display, 4-lane)

The SoC MIPI_DPHY1_TX (multiplexed with the DSI controller) has 4 data lanes + a clock pair routed to the connector DSI1 pin group. Per RK3588S Datasheet: DSI DPHY 2.0, up to 4.5 Gbps per lane, up to 4K@60 Hz, DSC 1.1/1.2a supported.

Connector Pin	Pin Name	Net (SoC Ball)
177 / 175	DSI1_D0_P/N	MIPI_DPHY1_TX_D0P/N (BB16/BA16)
183 / 181	DSI1_D1_P/N	MIPI_DPHY1_TX_D1P/N (BB17/BA17)
195 / 193	DSI1_D2_P/N	MIPI_DPHY1_TX_D2P/N (BA20/BB20)
196 / 194	DSI1_D3_P/N	MIPI_DPHY1_TX_D3P/N (BB22/BA22)
189 / 187	DSI1_C_P/N	MIPI_DPHY1_TX_CLKP/N (BB19/BA19)

Associated display control signals (via the GPIO table in Section 3.7): LCD_PWREN_H (GPIO7), LCD_RESET_L (GPIO8), LCD_BL_PWM (GPIO25).

3.10.2 MIPI CSI-2 CAM1 (4-lane)

The SoC MIPI_DPHY0_RX has 4 data lanes + a clock pair routed to the connector CAM1 pin group (per RK3588S Datasheet: CSI DPHY V1.2, 2.5 Gbps per lane).

Connector Pin	Pin Name	Net (SoC Ball)
117 / 115	CAM1_DO_P/N	MIPI_DPHY0_RX_D0P/N (BB38/BA38)
123 / 121	CAM1_D1_P/N	MIPI_DPHY0_RX_D1P/N (BA40/AY40)
135 / 133	CAM1_D2_P/N	MIPI_DPHY0_RX_D2P/N (AY42/BA42)
141 / 139	CAM1_D3_P/N	MIPI_DPHY0_RX_D3P/N (AW41/AW42)
129 / 127	CAM1_C_P/N	MIPI_DPHY0_RX_CLKP/N (BB41/BA41)

CAM1 associated signals:

Connector Pin	Pin Name	Net	Remarks
82 / 80	SDA0 / SCL0	I2C7_SDA/SCL_M2_CAM1	Camera I2C (SoC GPIO3_D3/GPIO3_D2, with pull-ups R95381/R95382)
97	CAM_GPIO	MIPI_DPHY_CSI_CAM1_RST_3V3	Reset output (SoC GPIO1_B2, 3.3 V)
55	GPIO14	MIPI_DPHY_CSI_CAM1_PDN_3V3	Power-Down output (SoC GPIO1_A6, 3.3 V)
51	GPIO15	MIPI_CSI_CAM1_CLKOUT	MCLK output (1.8 V at SoC side, level-shifted to 3.3 V via SN74LVC1T45 (U6))

3.10.3 MIPI CSI-2 CAM2 (2-lane)

The SoC MIPI_CSI0 (RX) has 2 data lanes + a clock pair routed to the connector USB3-0 pin group (pin multiplexing).

Connector Pin	Pin Name	Net (SoC Ball)
130 / 128	USB3-0-RX_P/N	MIPI_CSI0_RX_D0P/N (AL42/AL41)
136 / 134	USB3-0-D_P/N	MIPI_CSI0_RX_D1P/N (AK41/AK42)
142 / 140	USB3-0-TX_P/N	MIPI_CSI0_RX_CLK0P/N (AN42/AN41)

CAM2 associated signals:

Connector Pin	Pin Name	Net	Remarks
36 / 35	ID_SD / ID_SC	I2C5_SDA/SCL_M2_CAM2	Camera I2C (SoC GPIO4_A7/GPIO4_A6)
89	WL_NDISABLE	MIPI_DPHY_CSI_CAM2_RST_3V3	Reset output (SoC GPIO1_B3, 3.3 V)
91	BT_NDISABLE	MIPI_CSI_CAM2_CLKOUT_3V3	MCLK output (via R26, 3.3 V)
143	HDMI1_HOTPLUG	MIPI_DPHY_CSI_CAM2_PDN_3V3	Power-Down output (SoC GPIO4_B3, 3.3 V)

3.11 SDIO / eMMC

On-board eMMC (not routed to the connector): connected to the SoC GPIO2 multiplexed port via an 8-bit bus: EMMC_CLKOUT (GPIO2_A1), EMMC_CMD (GPIO2_A0), EMMC_D0–D7 (GPIO2_D0–D7), EMMC_DATA_STROBE (GPIO2_A2, DS), EMMC_RSTN (GPIO2_A3). Supplies: VCC = VCC_3V3_S3, VCCQ = VCC_1V8_S3 (see Chapter 6). Supports HS400/HS200/DDR50/legacy modes; bus width 1/4/8-bit (per RK3588S Datasheet).

Connector SDIO (SD card, 4-bit) — SDMMC0:

Connector Pin	Pin Name	Net (SoC Ball)	Remarks
57	SD_CLK	SDMMC_CLK (via R1320)	Clock
62	SD_CMD	SDMMC_CMD (GPIO4_D4)	Command
63 / 67 / 69 / 61	SD_DAT0/1/2/3	SDMMC_D0/D1/D2/D3 (GPIO4_D0–D3)	Data lines, 4-bit
75	SD_PWR_ON	SDMMC0_PWREN_H (GPIO4_B5)	SD card power enable output (carrier board controls card slot supply accordingly)
76	VBAT	SDMMC_DET_H (via R95602, inverted by Q24 to SDMMC_DET_L → SoC GPIO0_A4)	Pin multiplexing: the CM5 form factor VBAT pin is used as SD card detect in this design (active-high detect signal, level-inverted by Q24 to the SoC)
64 / 68 / 70 / 72	SD_DAT4/5/6/7	NC	Not used
73	SD_VDD_OVERRIDE	NC	Not used

SDIO is compatible with SD3.0 and MMC 4.51, 4-bit data width (per RK3588S Datasheet). The supply for the SDMMC0 pin level domain VCCIO_SD_S0 is specified in Chapter 6.

3.12 USB-C (CC1 / CC2)

Connector pins 94 / 96 (CC1 / CC2) are connected via resistor divider networks (R3/R4, R1/R2) to SoC SARADC_IN3 / IN4, allowing software to detect the carrier-board USB-C CC line states by ADC sampling (typical use: OTG role determination; specific thresholds and divider ratios **TBD**, refer to schematic and software implementation). The module contains no USB PD controller; Type-C CC resistors / PD negotiation are the responsibility of the carrier board.

3.13 Fan Control

Connector Pin	Pin Name	Net	Status
19	FAN_PWM	PWM14 / CAM3_CLK_M0 (via R42)	Available: SoC PWM14 output, usable for fan PWM speed control
16	FAN_TACHO	USB20_HOST0_DP	Unavailable: pin multiplexed as USB 2.0 Host0 data (see Section 3.6); fan tachometer input is not routed out

3.14 PMIC_EN / PWR_BUT

Connector Pin	Pin Name	Net	Connection	Remarks
99	PMIC_ENABLE	PWRON_L	RK806 PWRON	Power-key / shutdown control input (refer to Chapter 6 power-up sequencing)
92	PWR_BUT	PMIC_RESET_L	RK806 RESETB	Reset request input / PMIC reset output (refer to Chapter 6)

3.15 VBAT / RTC

- **VBAT pin multiplexing:** the CM5 form factor VBAT pin (76) is used as SD card detect input in this design (see Section 3.11).
- **RTC backup power:** provided via the connector **GPIO_VREF pin (78)**. The carrier-board input voltage is diode-ORed with the module-internal RTC supply rail through dual Schottky diode D2 (BAS70-05Q) to supply HYM8563TS (U1) (VCC_RTC). The permissible CM120 RTC backup input voltage range is **TBD** (refer to Section 4.3.2); the CM5 GPIO reference voltage range shall not be assumed to apply.
- **RTC:** HYM8563TS + 32.768 kHz crystal (Y1); I2C2 bus (SCL: SoC GPIO0_B7, SDA: GPIO0_C0, shared with RK860-3); RTC interrupt output RTC_INT_L → SoC GPIO0_B0; RTC 32 kHz output CLKOUT connected via R29/R28 to SoC GPIO0_B2 (RTC_32K_SOC). Operating temperature range and timekeeping accuracy **TBD** (refer to HYM8563 datasheet).

3.16 Boot Mode / Recovery

The RK3588S BootROM supports booting from eMMC, SD/MMC, and SPI, and supports system code download via USB OTG (per RK3588S Datasheet Section 1.2.2). The CM120 boot mode selection circuit is as follows:

Signal	Connection	Remarks
NRPIBOOT (connector pin 93)	Via divider network (R9202 / R1501 / R1502 / C1500) → SoC SARADC_IN0_BOOT	The carrier board pulls this pin up/down to change the SARADC sampled voltage, selecting eMMC boot or USB download (Maskrom) mode; threshold voltage TBD
SW1 (on-module pushbutton)	Paralleled to the NRPIBOOT divider node (via N21787389 / DR9200)	On-module Recovery pushbutton; functionally equivalent to the carrier board pulling NRPIBOOT low
KEY/RECOVERY	R1500 → SoC SARADC_IN1	On-module key detection channel (used in conjunction with the above; key-to-sample mapping per schematic)

3.17 LED

Connector Pin	Pin Name	Net	Driver	Remarks
21	PL_NLED_ACTIVITY	LED_GREEN_EN (via R75/R76)	SoC GPIO0_C5	Activity indicator LED (green, cathode drive)
95	NPL_LED_PWR	LED_RED_EN	SoC GPIO0_C4	Power indicator LED (red, cathode drive)

LED current-limiting resistor values, forward current, and brightness **TBD** (refer to schematic and carrier-board LED selection).

3.18 EEPROM_NWP / On-Board EEPROM

The module carries a BL24C16F (U90071, 16 Kbit I2C EEPROM, attached to the I2C0 bus, shared with the RK860-0/1 VSEL configuration) for storing module information (content format **TBD**). Its write-protect pin WP is controlled by SoC GPIO1_A7 (net PMW3_IR_M3, multiplex mode M3) via transistor Q2, with default pull-up R90619 to the write-inhibited state:

Connector Pin	Pin Name	Net	SoC Ball	Remarks
20	EEPROM_NWP	PMW3_IR_M3	GPIO1_A7	EEPROM write-protect control output (also available to the carrier board; logic cooperates with the Q2 network, refer to schematic)

Note: In the CM5 form factor, the ID_SD/ID_SC pins were originally intended for the carrier-board EEPROM; the CM120 multiplexes ID_SD/ID_SC as the CAM2 I2C (see Section 3.10.3).

3.19 Debug UART

The UART2_M0 debug console is routed to connector GPIO3/GPIO4:

Connector Pin	Pin Name	Net	SoC Ball	Direction
54	GPIO4	UART2_TX_M0_DEBUG	GPIO0_A6_z	Output (TXD)
56	GPIO3	UART2_RX_M0_DEBUG	GPIO0_A3_u	Input (RXD)

- The signals are routed out through ESD protection devices (D3/D4, ESD5311N) and series resistors (R7/R8).
- Baud rate and UART parameters **TBD** (subject to software default configuration; RK3588S UART supports up to 4 Mbps per Datasheet Section 1.2.13).

3.20 Other Low-Speed Interface Summary

I2C buses (the SoC provides 9 I2C controllers in total, per RK3588S Datasheet; module allocation as follows):

Bus	Purpose	Connector Pins	SoC Balls	Remarks
I2C0_M2	Module-internal: RK860-0/1 VSEL, BL24C16F EEPROM	—	GPIO0_D1/GPIO0_D2	Not routed out
I2C2_M0	Module-internal: RK860-2 (NPU supply VSEL), HYM8563 RTC	—	GPIO0_B7/GPIO0_C0	Not routed out
I2C5_M2	CAM2 camera	ID_SD (36) / ID_SC (35)	GPIO4_A7/GPIO4_A6	Routed out
I2C6_M0	Touch panel (TP)	GPIO22 (46) / GPIO10 (44)	GPIO0_C7/GPIO0_D0	Routed out, with pull-ups R43/R44
I2C7_M2	CAM1 camera	SDA0 (82) / SCL0 (80)	GPIO3_D3/GPIO3_D2	Routed out, with pull-ups R95381/R95382
PMIC bus	RK806 configuration	—	PMIC_SPI_MOSI/CLK/CS	SPI interface (not I2C)

SPI (the SoC provides 5 controllers):

Interface	Connector Pins	SoC Balls	Purpose
SPI4_M2 (CS0/CLK/MOSI/MISO)	GPIO12 (31) / GPIO21 (25) / GPIO20 (27) / GPIO16 (29)	GPIO1_A3/GPIO1_A2/GPIO1_A1/GPIO1_A0	General-purpose SPI routed out

I2S1 (audio, 8-channel controller, sampling rate up to 192 kHz, per RK3588S Datasheet):

Signal	Connector Pin	SoC Ball
I2S1_MCLK_M0	GPIO26 (24)	GPIO4_A0
I2S1_SCLK_M0	GPIO19 (26)	GPIO4_A1
I2S1_LRCK_M0	GPIO13 (28)	GPIO4_A2
I2S1_SDI0_M0	GPIO6 (30)	GPIO4_A5
I2S1_SDO0_M0	GPIO5 (34)	GPIO4_B1
I2S1_SDO1_M0	GPIO18 (49)	GPIO4_B2

UART / CAN: Besides UART2 (debug, Section 3.19), GPIO9/GPIO11 provide UART5 (M1) or CAN2 (M0) multiplexing (the RK3588S integrates three CAN 2.0B controllers; no CAN transceiver is populated on the module, so the carrier board shall provide one).

SARADC (12-bit, up to 1 MS/s, 6 single-ended input channels, per RK3588S Datasheet):

Channel	Net	Purpose
IN0_BOOT	SARADC_VIN0_BOOT	Boot mode sampling (NRPIBOOT / SW1, see Section 3.16)
IN1	SARADC_VIN1_KEY/RECOVERY	Key/recovery detection (see Section 3.16)
IN2	SARADC_VIN2_DC	TBD
IN3 / IN4	SARADC_VIN3 / SARADC_VIN4	CC1 / CC2 detection (see Section 3.12)
IN5	SARADC_VIN5	TBD

Other dedicated signals (connector):

Connector Pin	Pin Name	Net	Remarks
47	GPIO23	HP_DET_L	Headphone insertion detect input (active low)
48 / 50	GPIO27 / GPIO17	TP_INT_L / TP_RST_L	Touch panel interrupt / reset

3.21 Reset / Recovery Modes (Maskrom / Recovery)

The RK3588S supports Maskrom download mode (via USB OTG, see Section 3.16). System reset paths are: ① PWR_BUT → RK806 RESETB (Section 3.14); ② SoC internal software reset and watchdogs (the SoC integrates 5 watchdogs, per RK3588S Datasheet). If the carrier board requires hard-reset control, it may be implemented via GPIO or PMIC_ENABLE (design convention **TBD**).

3.22 Power Pins (Interface Side)

Connector Pin	Pin Name	Net	Direction	Remarks
77 / 79 / 81 / 83 / 85 / 87	5V_IN_1-6	VCC5V0_SYSIN	Input	Module main power input +5 V (six pins paralleled; connector rated 0.3 A / pin, aggregate limit 1.8 A ; recommended input 4.75 ~ 5.25 V, see Chapters 4 / 6)
84 / 86	3V3_O_1/2	VCC_3V3_S0	Output	Module 3.3 V output rail (for carrier-board IO use; load capability TBD)
88 / 90	1V8_O_1/2	VCC_1V8	Output	Module 1.8 V output rail (filtered from VCC_1V8_S3 via L2208/R39; load capability TBD)
78	GPIO_VREF	VRTC	Input	GPIO reference voltage input, also serving as RTC backup power (see Section 3.15)
1 / 2 / 7 / 8 / 13 / 14 / 22 / 23 / 32 / 33 / 42 / 43 / 52 / 53 / 59 / 60 / 65 / 66 / 71 / 72 / 74 / 98 / 107 / 108 / 113 / 114 / 119 / 120 / 125 / 126 / 131 / 132 / 137 / 138 / 143 / 144 / 150 / 155 / 156 / 161 / 162 / 167 / 168 / 173 / 174 / 179 / 180 / 185 / 186 / 191 / 192 / 197 / 198	GND1-GND51	GND	—	Signal ground / shield ground; mounting holes HOLE1-4 and shield pins A-H are also connected to GND

Power-up sequencing, power-down sequencing, power consumption, and individual rail specifications are detailed in Chapter 6 "Power".

4 Electrical and Mechanical

4.1 Mechanical

The CM120 adopts the Raspberry Pi Compute Module 5 mechanical form factor: all external interfaces are routed out through two 100-pin high-density board-to-board (BTB) connectors, and the carrier board mates with the module through the corresponding mating connectors.

4.1.1 Outline Dimensions

Per CM120_X10_20260910 dimensioned drawing (top/bottom view dimension drawing; vector-measured and calibrated against the 55.0 / 40.0 outline annotations):

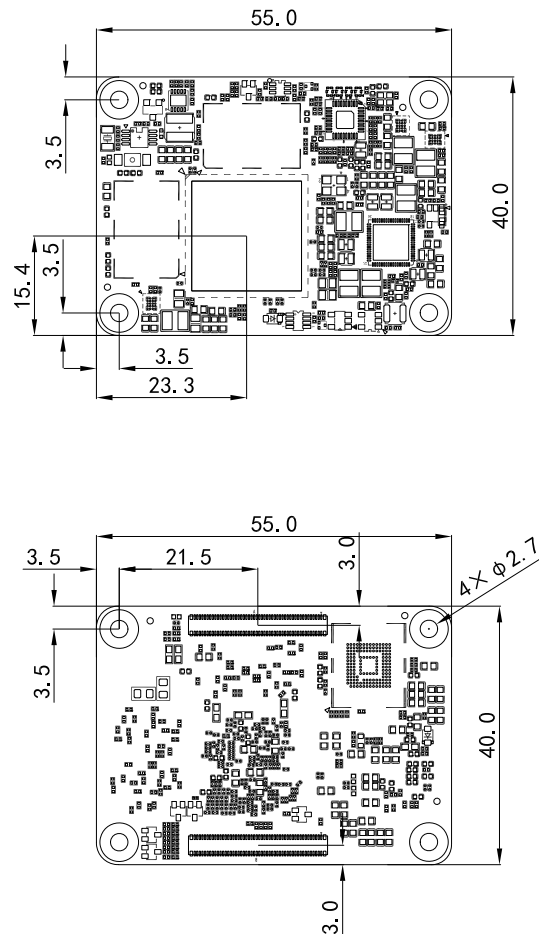


Figure 3: Radxa CM120 outline dimensions (top and bottom views)

Item	Value
Module outline (L × W)	55.0 mm × 40.0 mm
Mounting holes	4 × $\phi 2.7$ mm , hole centers 3.5 mm from each adjacent board edge (hole spacing 48.0 mm × 33.0 mm)
Connector placement (bottom side)	Two 100-pin connectors arranged along the 55 mm long edges: body length 21.5 mm , centerline 25.0 mm from the left board edge (3.5 + 21.5 annotation), centerlines 3.0 mm from the top / bottom board edges respectively, mirror-symmetric

Item	Value
SoC (RK3588S) position	Package center approximately 23.3 mm × 24.6 mm from board edges (top view, measured)
SoC (RK3588S) package	FCCSP1253L: body 17 mm × 17 mm, ball diameter 0.26 mm, ball pitch 0.4 mm

A complete 3D outline drawing with component height information is **TBD**.

4.1.2 Board-to-Board Connectors and Stacking Heights

Module-side connector (per BOM and Hirose DF40 series datasheet):

Item	Value	Reference
Connector quantity and type	2 × 100-pin high-density BTB connectors, 0.4 mm pitch	Netlist (U7, pins 1–100 / 101–200)
Module-side connector model	Hirose DF40C-100DP-0.4V(##) (Plug, Straight SMT; HRS P/N: CL0684-4032-1-##)	BOM / DF40 datasheet
Connector body dimensions	Length 21.52 mm (datasheet) / 21.5 mm (measured); width 3.38 mm class (series minimum depth 3.38 mm)	DF40 datasheet / dimensioned drawing
Rated current	0.3 A / pin (0.25 A for 120 pos)	DF40 datasheet, Product Specifications
Rated voltage	50 V AC/DC	Same as above
Contact resistance	≤ 90 mΩ (20 mV AC, 1 kHz, 1 mA)	Same as above
Insulation resistance / withstanding voltage	≥ 50 MΩ (100 V DC) / 150 V AC for 1 min, no flashover or breakdown	Same as above
Mating durability	30 cycles	Same as above
Operating temperature / humidity	–55 °C ~ +85 °C / 20 % ~ 80 % RH	Same as above
Vibration	10 ~ 55 Hz, single amplitude 0.75 mm, 2 h per 4-axis direction, no electrical discontinuity ≥ 1 μs	Same as above
Effective mating length	0.45 mm (at 1.5 mm stacking height)	DF40 datasheet, Features
Transmission capability	Supports USB4 Gen.2 (20 Gbps) transmission (H=1.5 mm type only)	Same as above

Carrier-side mating connectors and stacking heights (two options for DF40 series 100-pin, per the datasheet Stacking Height Variation table):

Stacking Height	Carrier-Side Mating Model (Receptacle)	HRS P/N	Remarks
1.5 mm	DF40C-100DS-0.4V(##)	CL0684-4033-4-##	0 mm clearance under module
3.0 mm	DF40HC(3.0)-100DS-0.4V(##)	CL0684-4151-0-##	1.5 mm clearance under module

⚠ **Stacking height difference from the CM5 ecosystem:** the official Raspberry Pi CM5 mating connectors are the Amphenol 10164227 series — 1.5 mm (10164227-1001A1RLF) and **4.0 mm** (10164227-1004A1RLF, 2.5 mm clearance) (CM5 Datasheet RP-008180-DS-7). The Hirose DF40 series 100-pin offers only **1.5 / 3.0 mm** stacking heights; the intermateability between the CM5 ecosystem 4.0 mm stacking connector and DF40C-100DP is **TBD** (until confirmed by Hirose / Amphenol documentation, carrier board designs shall use the DF40 mating models listed above).

3D model (STEP file): **TBD**.

4.1.3 Assembly and Layout Notes

1. **No wireless antenna clearance requirement:** the CM120 is not equipped with a wireless communication module (the WL_nDISABLE / BT_nDISABLE pins are multiplexed as CAM2 control signals, see Section 3.2); the requirements in the CM5 Datasheet regarding PCB antenna clearance, ground plane cutouts, and metal keep-out **do not apply to the CM120**.
2. **Connector current-carrying constraint:** the DF40C-100DP-0.4V is rated at **0.3 A / pin**. The +5V input uses six paralleled pins (pins 77–87), giving an aggregate connector rating of **1.8 A** (approximately 9 W at 5 V) — the carrier board +5V supply design shall not exceed this connector rating (power budget per Section 4.3.2 and Chapter 6).
3. The clearance height under the module (when mated) depends on the selected stacking height (see Section 4.1.2: 0 mm clearance at 1.5 mm stacking; 1.5 mm clearance at 3.0 mm stacking); component heights in that carrier-board area shall satisfy the mating requirements.
4. The mounting holes (4 × $\phi 2.7$ mm) and carrier-board mechanical fastening (standoff / screw specification) are recommended to be designed for M2.5 fasteners; carrier-board hole pattern and torque requirements **TBD**.
5. Mating durability is 30 cycles (DF40 datasheet); frequent mating in service / test scenarios shall be count-managed; during mating, utilize the connector self-alignment feature (± 0.33 mm, X/Y directions) and the 0.45 mm effective mating length; angled insertion is prohibited.

4.2 Thermal

4.2.1 Temperature Ranges

Item	Value	Reference
SoC junction temperature (absolute maximum)	125 °C	RK3588S Datasheet Table 3-1 (Tj), Section 4.1
SoC storage temperature	−40 °C ~ +125 °C	RK3588S Datasheet Table 3-1 (Tstg)
SoC recommended operating ambient temperature	0 °C ~ +80 °C	RK3588S Datasheet Table 3-2 (TA)
Module operating temperature range	TBD	Subject to system-level testing; jointly constrained by SoC, LPDDR4, eMMC, PHY, PMIC and all other devices (refer to respective datasheets)
Module storage temperature range	TBD	To be confirmed (SoC side: −40 ~ +125 °C)
Condensation	Not permitted (condensation shall be avoided during module operation and storage; details TBD)	—

4.2.2 SoC Package Thermal Characteristics

Thermal resistance characteristics of the RK3588S (FCCSP1253L package) are as follows (simulation reference values, subject to physical measurement; test conditions: 10-layer PCB, 200 mm × 130 mm, ambient temperature 25 °C):

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	θ_{JA}	8.2	°C/W
Junction-to-board thermal resistance	θ_{JB}	3.7	°C/W
Junction-to-case thermal resistance	θ_{JC}	0.01	°C/W

Reference: RK3588S Datasheet Table 4-1. These values are based on Rockchip-specified test board conditions; the equivalent thermal resistance under the CM120 actual PCB (layer count, dimensions, copper thickness **TBD**) and carrier-board thermal conditions shall be evaluated separately (**TBD**).

4.2.3 Temperature Monitoring and Protection

The RK3588S integrates a 7-channel temperature sensor (TS-ADC) with the following characteristics (RK3588S Datasheet Table 3-11):

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Measurement accuracy	Temp: -40 ~ 125 °C; Supply: 1.62 V ~ 1.98 V	—	±3	±5	°C
Sensing temperature range	—	-40	25	125	°C
Temperature resolution	—	—	1	—	°C

The TS-ADC supports user-defined mode and automatic mode: in automatic mode, the high/low temperature alarm interrupt temperatures and the system reset temperature are configurable (RK3588S Datasheet Section 1.2.14). The thermal throttling and over-temperature protection thresholds configured in the CM120 factory software are **TBD** (subject to software configuration definition).

4.2.4 Thermal Design Requirements

1. To ensure reliability and operating performance, the RK3588S junction temperature shall not exceed 125 °C under any operating condition (RK3588S Datasheet Section 4.1); when the junction temperature approaches the limit, the SoC will trigger alarms, frequency throttling, or reset according to the TSADC configuration (specific policy **TBD**).
2. For high ambient temperature or high load applications, the carrier board / end system shall provide a thermal solution for the module (heat sink, thermal pad, or forced air cooling; selection **TBD**); the relationship between permissible ambient temperature and typical power consumption without a thermal solution is **TBD** (subject to thermal testing).
3. The carrier-board thermal design shall also ensure that other devices on the module (LPDDR4, eMMC, RTL8211F-CG, RK806, RK860, etc.) remain within the operating temperature ranges specified in their respective datasheets (device limits **TBD**, refer to respective datasheets).

4.3 Electrical Specification

⚠ **WARNING:** Stresses beyond the ratings listed in the table below may cause permanent damage to the device. These are stress ratings only and do not imply functional operation of the device at these or any other conditions beyond the recommended op-

erating conditions. Prolonged exposure to absolute maximum rating conditions may affect device reliability.

4.3.1 Absolute Maximum Ratings (Module Level)

Symbol	Parameter	Min.	Max.	Unit	Reference / Remarks
V5V_IN	5V_IN pin (77/79/81/83/85/87) input voltage	−0.3	7.0	V	JW5265 Datasheet absolute maximum ratings (PVIN/SVIN pins −0.3 ~ 7 V); the RK806 OVLO 6.0 V trip point is below this value, >6 V will trigger protective shutdown (see Section 6.7)
VGPI0_33	Connector GPIO pin voltage (pins in 1.8 V/3.3 V dual-rail voltage domains)	−0.5	3.63	V	RK3588S Table 3-1 (PMUIO2 / VCCIO2 / VCCIO4 / VCCIO5 / VCCIO6 domains)
VGPI0_18	Connector GPIO pin voltage (pins in 1.8 V-only voltage domains)	−0.5	1.98	V	RK3588S Table 3-1 (PMUIO1 / VCCIO1 / EMMCIO domains)
VGPI0_VREF	GPIO_VREF pin (78, RTC backup power input) voltage	TBD	TBD	V	Determined by the input ranges of D2 (BAS70-05Q) and HYM8563TS; refer to respective datasheets
V3V3_O / V1V8_O	3V3_O / 1V8_O output pin voltage	TBD	TBD	V	Determined by RK806 PLDO outputs and SGM2590 load switch specifications; refer to respective datasheets
Tstg	Module storage temperature	TBD	TBD	°C	To be confirmed (SoC side: −40 ~ +125 °C)
Tj	SoC junction temperature	—	125	°C	RK3588S Table 3-1
ESD	Electrostatic discharge tolerance (HBM/CDM)	TBD	TBD	—	Subject to testing or aggregation of device specifications

Note: The voltage domain of each connector GPIO pin is specified in Section 4.3.2; **some connector GPIOs are located in 1.8 V-only voltage domains** (per RK3588S Table 3-1/3-2, PMUIO1, VCCIO1, and EMMCIO are 1.8 V-only supply domains). Level compatibility shall be verified before direct connection from the carrier board (pin-by-pin assignment **TBD**, see Section 3.7 and RK3588S pin documentation).

4.3.2 Recommended Operating Conditions

Module level:

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remarks
V5V_IN	5V_IN main power input voltage	4.75	5.0	5.25	V	Consistent with the CM5 form factor (CM5 DS: 4.75 ~ 5.25 V); within the JW5265 input range (2.5 ~ 6 V) and the RK806 OVLO (6.0 V) / UVLO (2.7 V) window; the 5 V rail shall rise monotonically to ≥4.75 V and remain above this level
I5V_IN	5V_IN input current	—	TBD	1.8	A	Six pins paralleled; the upper limit is constrained by the DF40C-100DP-0.4V rating of 0.3 A / pin (6 × 0.3 A, see Section 4.1.3)
VGPI0_VREF	GPIO_VREF (pin 78) input voltage	TBD	3.0 (reference)	TBD	V	Used as RTC backup power (via D2 diode OR-ing); the CM5 form factor defines this pin as a 1.8 V / 3.3 V input; the actual permissible range for CM120 is TBD
TA	Module operating ambient temperature	TBD	—	TBD	°C	SoC side recommended 0 ~ 80 °C (RK3588S Table 3-2); module level subject to testing
fOSC	SoC input clock	—	24	—	MHz	On-board 24 MHz crystal (RK3588S Table 3-2: OSC input clock frequency 24 MHz; crystal model TBD)

Key difference from CM5: On the CM5, the GPIO_VREF pin supplies the GPIO0–GPIO27 bank (1.8 V or 3.3 V, selectable but shall not be left floating). **On the CM120, this pin is not used to supply GPIO banks** — the voltage domains of the module connector GPIOs are supplied by module-internal power rails (see table below), and GPIO_VREF serves only as the RTC backup power input.

GPIO voltage domains (SoC power domain ↔ module supply network mapping, per netlist):

SoC Power Domain	Domain Type (RK3588S Table 3-1/3-2)	Module Supply Network	Supply Source	Remarks
PMUIO1_1V8	1.8 V only	VCC1V8_PMU_DDR_S3	TBD (RK806 output, see Chapter 6)	This network also supplies LPDDR4 VDD1
PMUIO2_1V8 + PMUIO2 (3V3 balls)	1.8 V / 3.3 V	VCC1V8_PMU_DDR_S3 (1V8 balls) + VCC_3V3_S3 (3V3 balls)	Dual-rail connection	Both rails connected; the actual IO level selection mechanism is TBD (software IO domain configuration, refer to software documentation)
VCCIO1_1V8	1.8 V only	VCC_1V8_S0	RK806 PLDO2	—
VCCIO2_1V8 + VCCIO2 (3V3 balls)	1.8 V / 3.3 V	VCC_1V8_S0 (1V8 balls) + VCCIO_SD_S0 (3V3 balls)	RK806 PLDO5 (VCCIO_SD_S0)	VCCIO_SD_S0 is the SD IO supply rail (voltage switching capability TBD , subject to RK806 configuration)
EMMCIO_1V8	1.8 V only	VCCIO_FLASH (via R4000 from VCC_1V8_S3)	RK806 VOUT10	On-board eMMC IO, 1.8 V
VCCIO4_1V8 + VCCIO4 (3V3 balls)	1.8 V / 3.3 V	VCC_1V8_S0 (1V8 balls) + VCC_3V3_S0 (3V3 balls)	RK806 PLDO2 / SGM2590 (U3)	Dual-rail connection; VCC_3V3_S0 also feeds the 3V3_O pins
VCCIO5_1V8 + VCCIO5 (3V3 balls)	1.8 V / 3.3 V	VCC_1V8_S0 + VCC_3V3_S0	Same as above	Same as above
VCCIO6_1V8 + VCCIO6 (3V3 balls)	1.8 V / 3.3 V	VCC_1V8_S0 + VCC_3V3_S0	Same as above	Same as above
DDR IO (VDDQ)	LPDDR4: 0.6 V	VDDQ_DDR_S0	RK806 VOUT9	LPDDR4 VDDQ (RK3588S Table 3-2: 0.57 ~ 0.63 V)

- The pin-by-pin correspondence between GPIO banks and SoC power domains is subject to RK3588S Datasheet pin documentation (the V1.4 ball list on which this document is based does not contain a power domain column; pin-by-pin assignment **TBD**). The RK3588S ball name suffixes **_u/ _d/ _z** are SoC IO voltage domain markers (definitions per RK3588S pin description documentation).
- The 26 connector GPIO bits (table in Section 3.7) are distributed across SoC GPIO0 / GPIO1 / GPIO3 / GPIO4 banks; pins located in 1.8 V-only domains (PMUIO1 / VCCIO1) shall not be driven with 3.3 V levels by the carrier board (pin-by-pin assignment **TBD**, must be verified).
- The actual IO level of dual-rail domains (1.8 V/3.3 V) is selected by software configuration; the factory default configuration is **TBD**.

4.3.3 GPIO DC Characteristics

The following tables give the DC characteristics of the connector GPIOs (RK3588S digital general-purpose IOs), per RK3588S Datasheet Table 3-3 / 3-4. VDDO / DVDD denotes the

IO supply voltage (i.e., the actual level of the corresponding voltage domain in the Section 4.3.2 table).

GPIOs in 1.8 V / 3.3 V dual-rail voltage domains (PMUIO2 / VCCIO2 / VCCIO4 / VCCIO5 / VCCIO6):

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input low level	VIL	VDDO = 3.3 V or 1.8 V	VSS	—	$0.3 \times VDDO$	V
Input high level	VIH	Same as above	$0.7 \times VDDO$	—	VDDO	V
Output low level	VOL	—	VSS	—	$0.25 \times DVDD$	V
Output high level	VOH	—	$0.75 \times DVDD$	—	DVDD	V
Internal pull-up resistance	RPU	@3.3 V	10	—	100	kΩ
Internal pull-down resistance	RPD	@3.3 V	10	—	100	kΩ
Internal pull-up resistance	RPU	@1.8 V	10	—	50	kΩ
Internal pull-down resistance	RPD	@1.8 V	10	—	50	kΩ
Schmitt trigger hysteresis	VH	@3.3 V	$0.08 \times VDDO$	—	—	V
Schmitt trigger hysteresis	VH	@1.8 V	$0.1 \times VDDO$	—	—	V
Input leakage current	IPAD	VDD = DMAX, VPAD = 0 V	–10	—	10	μA
Pull-up resistor current	IRPU	@3.3 V / 1.8 V, VPAD = 0 V	–180	—	–20	μA
Pull-down resistor current	IRPD	@3.3 V / 1.8 V, VPAD = VDDO	20	—	180	μA

GPIOs in 1.8 V-only voltage domains (PMUIO1 / VCCIO1):

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input low level	VIL	VDDO = 1.8 V	VSS	—	$0.3 \times VDDO$	V
Input high level	VIH	VDDO = 1.8 V	$0.7 \times VDDO$	—	VDDO	V
Output low level	VOL	—	VSS	—	$0.25 \times DVDD$	V
Output high level	VOH	—	$0.75 \times DVDD$	—	DVDD	V
Internal pull-up/pull-down resistance	RPU / RPD	@1.8 V	10	—	50	kΩ
Schmitt trigger hysteresis	VH	@1.8 V	$0.1 \times VDDO$	—	—	V
Input leakage current	IPAD	VDD = DMAX, VPAD = 0 V	–10	—	10	μA
Pull-up resistor current	IRPU	VPAD = 0 V	–170	—	–20	μA
Pull-down resistor current	IRPD	VPAD = VDDO	20	—	170	μA

On-board eMMC IO (EMMCIO domain, 1.8 V, module-internal, not routed to connector):

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input low level	VIL	—	—	$0.35 \times DVDD$	V
Input high level	VIH	$0.65 \times DVDD$	—	—	V
Output low level	VOL	—	—	0.45	V
Output high level	VOH	$DVDD - 0.45$	—	—	V
Internal pull-up/pull-down resistance	RPU / RPD	10	—	50	kΩ

Drive capability note: RK3588S GPIO drive strength is configurable (RK3588S Datasheet Section 1.2.14); however, the V1.4 datasheet does not provide a graded drive-current table in the form of CM5 Datasheet Table 3 (IOL/IOH @ 2/4/8/12 mA). The available drive current of each CM120 GPIO is **TBD** (subject to RK3588S supplementary documentation or measurement). Until such data is obtained, carrier board

designs shall not design loads based on the CM5 drive current values.

4.3.4 High-Speed Interface Transmit/Receive Electrical Characteristics (PCIe 2.1 / SATA 3.0 Combo PIPE PHY)

The two PCIe 2.1 ×1 lanes on the CM120 connector (including Channel B multiplexed on the USB3-1 pin group) and the USB3.1/DP multiplexed channel are all provided by RK3588S Combo PIPE PHYs. Their transmit/receive DC/AC parameters are as follows (RK3588S Datasheet Table 3-8):

Transmitter (TX):

Parameter	Symbol	Min.	Typ.	Max.	Unit
Differential peak-peak output swing	VTX_DIFF_PP	800	1000	1200	mV
Low-power differential peak-peak output swing	VTX_DIFF_PP_LOW	400	—	1200	mV
Output differential impedance	RTX_DIFF_DC	80	100	120	Ω
Single-ended output resistance mismatch	RTX_DC_OFFSET	—	—	5	%
Output common-mode voltage	VTX_DC_CM	400	—	800	mV
TXP/TXM maximum timing and amplitude mismatch	VTX_CM_AC_PP_ACTIVE	—	—	50	mV
Allowed voltage change during receiver detection	VTX_RCV_DETECT	—	—	600	mV
De-emphasis	VTX_DE_RATIO	3.0	3.5	4.0	dB
AC coupling capacitor (USB3.1/PCIe)	CAC_COUPLING	75	—	200	nF
AC coupling capacitor (SATA)	CAC_COUPLING	6	—	12	nF
Rise time (20%–80%)	Tr	25	—	—	ps
Fall time (20%–80%)	Tf	25	—	—	ps
Transmitter short-circuit current limit	ITX_SHORT	—	—	20	mA
Output differential skew	TSKEW_DIFF	–15	—	15	ps

Receiver (RX):

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage swing	VRXDPP_C	250	—	1200	mVpp
Input differential impedance	RRXD_C	80	100	120	Ω
Single-ended input resistance mismatch	RRXD_C_MS	—	—	5	%

PHY electrical characteristics of other interfaces are directly referenced from RK3588S Datasheet Chapter 3:

Interface	Specification Table	Key Parameters (Excerpted)
MIPI C-PHY (D-PHY combo)	Table 3-9	LP-RX: $V_{IH} \geq 880 \text{ mV}$, $V_{IL} \leq 550 \text{ mV}$
MIPI CSI D-PHY (RX)	Table 3-10	Common-mode interference, pulse rejection and other receive tolerance parameters (refer to the original table)

Interface	Specification Table	Key Parameters (Excerpted)
SARADC (NRPIBOOT / CC detection / KEY sampling)	Table 3-10	12-bit resolution; analog input range AVSS18 ~ AVDD18 (1.8 V); DNL ± 1.0 (typ) / ± 3.0 (max) LSB; INL ± 2.0 (typ) / ± 6.0 (max) LSB ($F_s = 1$ MS/s, FCLK = 20 MHz)
TS-ADC	Table 3-11	See Section 4.2.3
PLL (INT/FRAC/DDR)	Table 3-5/3-6/3-7	E.g., INT PLL: output 35.2 ~ 4500 MHz, VCO 2250 ~ 4500 MHz, lock time ≤ 150 cycles (refer to the original table)
DDR IO	Table 3-3	$V_{IL} \leq V_{ref} - 0.14$ V, $V_{IH} \geq V_{ref} + 0.14$ V, $V_{OL} \leq 0.2$ V, $V_{OH} \geq 0.25$ V, $I_{IL}/I_{IH} \pm 100$ μ A (room temperature) / ± 500 μ A (high temperature)
USB 2.0 / HDMI / eDP / MIPI DSI	—	Per respective specifications (USB 2.0, HDMI 2.1 / FRL, eDP 1.3, MIPI D-PHY 2.0); SoC-side parameters per RK3588S Datasheet

4.3.5 Module-Internal Power Architecture Overview

Major internal power networks and sources (per netlist):

Power Network	Source	Design Nominal	Main Loads
VCC_SYSIN	JW5265 (U2) SW, via L1 (1.5 μ H)	4.04 V (VFB = 0.6 V, divider R18 47 k Ω / R21 8.2 k Ω : $0.6 \times (1 + 47/8.2) = 4.039$ V)	RK806 / 3 $\times$ RK860 / SY8089 inputs
VDD_CPU_BIG0_S0	RK860 (U2300) VOUT	0.55 ~ 1.05 V adjustable (RK3588S T3-2)	SoC CPU BigCore0 (incl. MEM balls)
VDD_CPU_BIG1_S0	RK860 (U2301) VOUT	0.55 ~ 1.05 V adjustable (RK3588S T3-2)	SoC CPU BigCore1
VDD_NPU_S0	RK860 (U2302) VOUT	0.55 ~ 0.95 V adjustable (RK3588S T3-2)	SoC NPU (incl. MEM balls)
VDD_CPU_LIT_S0	RK806 VOUT2 (SW2/L2203)	0.55 ~ 0.95 V (RK3588S T3-2)	SoC CPU LitCore (incl. MEM balls)
VDD_GPU_S0	RK806 VOUT1 (SW1/L2201)	0.55 ~ 0.95 V (RK3588S T3-2)	SoC GPU (incl. MEM balls)
VDD_LOGIC_S0	RK806 VOUT3 (SW3/L2205)	0.675 ~ 0.825 V (RK3588S T3-2)	SoC core logic
VDD_VDENC_S0	RK806 VOUT4 (SW4/L2207)	0.675 ~ 0.825 V (RK3588S T3-2)	SoC VCODEC (incl. MEM balls)
VDD_DDR_S0	RK806 VOUT5 (SW5/L2200)	0.675 ~ 0.85 V (RK3588S T3-2)	SoC DDR CH0/CH1 logic and MIF
VDD2_DDR_S3	RK806 VOUT6 (SW6/L2202)	0.85 V domain (RK3588S T3-2: 0.675 ~ 0.935 V)	LPDDR4 $\times 2$ VDD2 (always-on rail)

Power Network	Source	Design Nominal	Main Loads
VCC_3V3_S3	RK806 VOUT8 (SW8/L2206)	3.3 V	eMMC VCC, PMUIO2 3V3 balls, SGM2590 input, RTC OR-ing (D2)
VCC_1V8_S3	RK806 VOUT10 (SW10/L2208)	1.8 V	eMMC VCCQ, PMUIO domains (VCC1V8_PMU_DDR_S3), 1V8_O pins (via R39/R40)
VDDQ_DDR_S0	RK806 VOUT9 (SW9/L2204)	0.6 V (LPDDR4 VDDQ, RK3588S T3-2: 0.57 ~ 0.63 V)	SoC DDR VDDQ, LPDDR4 VDDQ
VDDQ_DDR_CKE_S3	VDD2_DDR_S3 via R3820	LPDDR4 CKE retention domain (RK3588S T3-2: 1.045 ~ 1.155 V)	SoC DDR VDDQ_CKE
VCC_3V3_S0	SGM2590 (U3) load switch, input VCC_3V3_S3	3.3 V (switchable)	VCCIO4/5/6 3V3 balls, 3V3_O pins, EEPROM, etc.
VCC_1V8_S0	RK806 PLDO2	1.8 V	VCCIO1/2/4/5/6 1V8 balls, etc.
VCCA_1V8_S0	RK806 PLDO1	1.8 V	SoC analog (PLL/PHY/HDMI/USB AVDD)
VDDA_1V2_S0	RK806 PLDO3	1.2 V	MIPI D/C PHY VDD_1V2
VCCA_3V3_S0	RK806 PLDO4	3.3 V	USB20 AVDD_3V3, etc.
VCCIO_SD_S0	RK806 PLDO5	1.8 V / 3.3 V switchable (TBD)	SoC VCCIO2 (3V3 balls), SD IO
VDD_0V75_S3	RK806 NLDO1	0.75 V (RK3588S T3-2)	SoC PMU_0V75
VDDA_0V75_S0	RK806 NLDO3	0.75 V (RK3588S T3-2)	SoC CSI DPHY/PLL/USB/OTP analog
VDDA_0V85_S0	RK806 NLDO4	0.85 V (RK3588S T3-2)	SoC Combo PIPE PHY / DP analog
HDMI_VDDA0V85_S0	RK806 NLDO5	0.75 V (RK3588S T3-2)	SoC HDMI/eDP TX0 analog
VDDA_DDR_PLL_S0	RK806 NLDO2	0.85 V domain (RK3588S T3-2)	SoC DDR PLL
VCC_RTC	D2 (BAS70-05Q) OR-ing: GPIO_VREF (pin 78) or VCC_3V3_S3	TBD	HYM8563TS VDD

The actual voltages of the RK806 output rails are configured by PMIC firmware via the SPI bus (PMIC_SPI_MOSI/CLK/CS); the RK860 rails are configured via I2C0/I2C2. Factory configuration values are **TBD** (subject to power design calculations and firmware configuration confirmation).

4.3.6 Power Consumption

Module power consumption is highly application-dependent; the values in the table below are subject to system-level measurement (**all TBD**):

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_SHUTDOWN_0	Shutdown current	PMIC_ENABLE (pin 99) = 0 V	—	TBD	—	mA
I_SHUTDOWN_2	Shutdown current	PMIC_ENABLE > 2 V	—	TBD	—	mA
I_IDLE	Idle current	PMIC_ENABLE > 2 V, system idle	—	TBD	—	mA
I_LOAD	Operating load current	PMIC_ENABLE > 2 V, typical load	—	TBD	—	mA
I_LOAD_MAX	Peak current	Full load (CPU/GPU/NPU fully loaded)	—	TBD	—	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_VRTC_OFF	RTC backup input current (module powered off)	Supplied via GPIO_VREF (pin 78)	—	TBD	—	μA
I_VRTC_ON	RTC supply current (module running)	—	—	TBD	—	μA

The RTC backup current is determined by the HYM8563TS and its peripherals (32.768 kHz crystal); refer to the HYM8563TS datasheet (**TBD**).

5 Pinout

All external electrical interfaces of the CM120 are routed out through two 100-pin high-density board-to-board (BTB) connectors. In the schematic and netlist they are represented by a single connector symbol **U7** (reference designator), with pins 1–100 corresponding to the first connector and pins 101–200 to the second; there are additionally 4 mounting holes (201–204) and 8 shield/ground pins (A–H). The module-side connector model is **Hirose DF40C-100DP-0.4V** (Plug, 0.4 mm pitch, Straight SMT, HRS P/N CL0684-4032-1-##), rated at **0.3 A / pin**, 50 V AC/DC, with a mating durability of 30 cycles; carrier-side mating connectors: **DF40C-100DS-0.4V** (CL0684-4033-4-##) for 1.5 mm stacking, or **DF40HC(3.0)-100DS-0.4V** (CL0684-4151-0-##) for 3.0 mm stacking (see Section 4.1.2 for details).

Table Conventions

- The **Signal Name** column follows the connector pin naming of the Raspberry Pi CM5 form factor (consistent with CM5 Datasheet Table 5) to ensure comparability of carrier board design documentation.
- The **CM120 Actual Function** column states the module-internal net and actual usage verified by the netlist. **Where the two differ (multiplexed/redefined pins), the “CM120 Actual Function” column prevails and is marked with Δ** (see the Interfaces chapter for the corresponding interface descriptions).
- “SoC Ball” denotes the RK3588S (U1000, FCCSP1253L package) ball coordinate; other devices such as the network transformer and PHY are identified by reference designator.
- Directions are referenced to the module: I = input (carrier → module), O = output (module → carrier), I/O = bidirectional, P = power, — = not applicable.

5.1 Pin Definitions (Pins 1–100, First Connector)

Table 51: Pin definitions (pins 1–100, first connector)

Pin	Signal Name (CM5-Compatible)	Dir.	CM120 Actual Function (Net)	Description
1	GND	—	GND	Ground (0 V)
2	GND	—	GND	Ground (0 V)
3	Ethernet_Pair3_P	I/O	PHY1_MDI3+	Gigabit Ethernet differential pair 3 positive; via on-board network transformer to RTL8211F PHY (U9) MDI3+ (100 Ω differential pair)
4	Ethernet_Pair1_P	I/O	PHY1_MDI1+	Ethernet differential pair 1 positive → U9 MDI1+
5	Ethernet_Pair3_N	I/O	PHY1_MDI3–	Ethernet differential pair 3 negative → U9 MDI3–
6	Ethernet_Pair1_N	I/O	PHY1_MDI1–	Ethernet differential pair 1 negative → U9 MDI1–
7	GND	—	GND	Ground (0 V)
8	GND	—	GND	Ground (0 V)
9	Ethernet_Pair2_N	I/O	PHY1_MDI2–	Ethernet differential pair 2 negative → U9 MDI2–
10	Ethernet_Pair0_N	I/O	PHY1_MDI0–	Ethernet differential pair 0 negative → U9 MDI0–
11	Ethernet_Pair2_P	I/O	PHY1_MDI2+	Ethernet differential pair 2 positive → U9 MDI2+

Pin	Signal Name (CM5-Compatible)	Dir.	CM120 Actual Function (Net)	Description
12	Ethernet_Pair0_P	I/O	PHY1_MDIO+	Ethernet differential pair 0 positive → U9 MDIO+
13	GND	—	GND	Ground (0 V)
14	GND	—	GND	Ground (0 V)
15	Ethernet_nLED3	O	PHY_YLED-	RTL8211F yellow LED output (3.3 V, active low); link speed/activity indication; drive capability and polarity configuration see 3.3 (TBD)
16	Fan_Tacho	I/O	△ USB2.0 Host0 D+ (USB20_HOST0_DP, SoC ball AW6)	Multiplexed: the CM5 fan tachometer input is the USB2.0 Host0 High-Speed data pair positive in this design (90 Ω differential pair)
17	Ethernet_nLED2	O	PHY_GLED+	RTL8211F green LED output (3.3 V); link/activity indication, see 3.3
18	Ethernet_SYNC_OUT	I/O	△ USB2.0 Host0 D- (USB20_HOST0_DM, AV6)	Multiplexed: forms the USB2.0 Host0 differential data pair together with pin 16
19	Fan_PWM	O	PWM14/CAM3_CLK_M0 (via R42)	Fan PWM speed-control output (SoC PWM14, multiplexed with CAM3_MCLK, mode M0); 3.3 V, duty-cycle control
20	EEPROM_nWP	O	PMW3_IR_M3 (SoC GPIO1_A7)	On-board EEPROM (U90071) write-protect control output, driven via transistor Q2, R90619 default pull-up to write-inhibited state; level domain see Note 4 (GPIO1)
21	LED_nACT	O	LED_GREEN_EN (via R75/R76 transistor circuit)	Active-low activity indicator LED drive output (corresponds to CM5 LED_nACT function)
22	GND	—	GND	Ground (0 V)
23	GND	—	GND	Ground (0 V)
24	GPIO26	I/O	I2S1_MCLK_M0 (SoC GPIO4_A0)	General-purpose GPIO; default multiplex I2S1 master clock (audio MCLK, see 3.8/3.11)
25	GPIO21	I/O	△ SPI4_CLK_M2 (SoC GPIO1_A2)	General-purpose GPIO; default multiplex SPI4 clock. GPIO1 bank, level domain see Note 4
26	GPIO19	I/O	I2S1_SCLK_M0 (SoC GPIO4_A1)	General-purpose GPIO; default multiplex I2S1 bit clock
27	GPIO20	I/O	△ SPI4_MOSI_M2 (SoC GPIO1_A1)	General-purpose GPIO; default multiplex SPI4 MOSI. GPIO1 bank, see Note 4
28	GPIO13	I/O	I2S1_LRCK_M0 (SoC GPIO4_A2)	General-purpose GPIO; default multiplex I2S1 frame clock
29	GPIO16	I/O	△ SPI4_MISO_M2 (SoC GPIO1_A0)	General-purpose GPIO; default multiplex SPI4 MISO. GPIO1 bank, see Note 4
30	GPIO6	I/O	I2S1_SDI0_M0 (SoC GPIO4_A5)	General-purpose GPIO; default multiplex I2S1 data input 0
31	GPIO12	I/O	△ SPI4_CS0_M2 (SoC GPIO1_A3)	General-purpose GPIO; default multiplex SPI4 chip select 0. GPIO1 bank, see Note 4
32	GND	—	GND	Ground (0 V)
33	GND	—	GND	Ground (0 V)
34	GPIO5	I/O	I2S1_SDO0_M0 (SoC GPIO4_B1)	General-purpose GPIO; default multiplex I2S1 data output 0
35	ID_SC	I/O	△ I2C5_SCL_M2_CAM2 (SoC GPIO4_A6)	Multiplexed: the CM5 HAT EEPROM identity bus is the CAM2 camera I ² C clock in this design; on-board R6 pull-up to 3.3 V
36	ID_SD	I/O	△ I2C5_SDA_M2_CAM2 (SoC GPIO4_A7)	Multiplexed: CAM2 camera I ² C data; on-board R13 pull-up to 3.3 V
37	GPIO7	O	△ LCD_PWREN_H (SoC GPIO1_A4)	General-purpose GPIO; default function LCD panel power enable (active high). GPIO1 bank, see Note 4
38	GPIO11	I/O	UART5_RX_M1 / CAN2_TX_M0 (SoC GPIO3_C5)	General-purpose GPIO; default multiplex UART5 receive / CAN2 transmit
39	GPIO8	O	△ LCD_RESET_L (SoC GPIO1_B0)	General-purpose GPIO; default function LCD reset (active low). GPIO1 bank, see Note 4
40	GPIO9	I/O	UART5_TX_M1 / CAN2_RX_M0 (SoC GPIO3_C4)	General-purpose GPIO; default multiplex UART5 transmit / CAN2 receive
41	GPIO25	O	△ LCD_BL_PWM (SoC GPIO1_B1)	General-purpose GPIO; default function LCD backlight PWM. GPIO1 bank, see Note 4
42	GND	—	GND	Ground (0 V)
43	GND	—	GND	Ground (0 V)
44	GPIO10	I/O	I2C6_SCL_M0_TP (SoC GPIO0_D0)	General-purpose GPIO; default multiplex touch panel I ² C clock; on-board R44 pull-up to 3.3 V
45	GPIO24	O	OTG0_PWREN_H (SoC GPIO3_D5)	General-purpose GPIO; default function OTG port power enable (active high)
46	GPIO22	I/O	I2C6_SDA_M0_TP (SoC GPIO0_C7)	General-purpose GPIO; default multiplex touch panel I ² C data; on-board R43 pull-up to 3.3 V
47	GPIO23	I	HP_DET_L (SoC GPIO3_D4)	General-purpose GPIO; default function headphone detect (active low)
48	GPIO27	I	△ TP_INT_L (SoC GPIO1_B5)	General-purpose GPIO; default function touch panel interrupt (active low). GPIO1 bank, see Note 4
49	GPIO18	I/O	I2S1_SDO1_M0 (SoC GPIO4_B2)	General-purpose GPIO; default multiplex I2S1 data output 1
50	GPIO17	O	△ TP_RST_L (SoC GPIO1_B4)	General-purpose GPIO; default function touch panel reset (active low). GPIO1 bank, see Note 4
51	GPIO15	O	△ MIPI_CSI_CAM1_CLKOUT_1V8 (via U6 level-shifter network)	Multiplexed: CAM1 camera MCLK output; net name marked 1V8, actual output level subject to schematic (TBD, see TBD-10 at end of chapter)
52	GND	—	GND	Ground (0 V)
53	GND	—	GND	Ground (0 V)
54	GPIO4	O	UART2_TX_M0_DEBUG	General-purpose GPIO; multiplexed as debug UART TX (UART2_M0, 115200-8-N-1 default, see 3.21)

Pin	Signal Name (CM5-Compatible)	Dir.	CM120 Actual Function (Net)	Description
55	GPIO14	O	△ MIPI_DPHY_CSI_CAM1_PDN_3V3 (SoC GPIO1_A6)	Multiplexed: CAM1 Power-Down control (3.3 V output). GPIO1 bank, see Note 4
56	GPIO3	I	UART2_RX_M0_DEBUG	General-purpose GPIO; multiplexed as debug UART RX (UART2_M0)
57	SD_CLK	O	SDMMC_CLK (SoC SDMMC0 controller, via series resistor R1320)	SD card interface clock (SDR25/SDR50 default TBD)
58	GPIO2	I	△ USBCC_INT_L (SoC GPIO4_A4)	General-purpose GPIO; multiplexed as carrier-side USB-C controller interrupt input (active low)
59	GND	—	GND	Ground (0 V)
60	GND	—	GND	Ground (0 V)
61	SD_DAT3	I/O	SDMMC_D3	SD card data 3 (SoC SDMMC0)
62	SD_CMD	I/O	SDMMC_CMD	SD card command/response (via series resistor network, refer to schematic)
63	SD_DAT0	I/O	SDMMC_D0	SD card data 0
64	SD_DAT5	—	NC	Not connected (the CM5Lite 8-bit bus bit is not used in this design)
65	GND	—	GND	Ground (0 V)
66	GND	—	GND	Ground (0 V)
67	SD_DAT1	I/O	SDMMC_D1	SD card data 1
68	SD_DAT4	—	NC	Not connected
69	SD_DAT2	I/O	SDMMC_D2	SD card data 2
70	SD_DAT7	—	NC	Not connected
71	GND	—	GND	Ground (0 V)
72	SD_DAT6	—	NC	Not connected
73	SD_VDD_OVERRIDE	—	NC	Not connected (the CM5 SD 1.8 V override function is not provided in this design; the SDIO signal level is determined by module-internal supplies, see 3.12)
74	GND	—	GND	Ground (0 V)
75	SD_PWR_ON	O	SDMMC0_PWREN_H (SoC GPIO4_B5)	SD card power enable output (active high); the carrier board controls the card slot supply switch accordingly
76	VBAT	I	△ SDMMC_DET_H (pulled up via R95602, inverted by Q24 to SoC GPIO0_A4)	Multiplexed: the CM5 RTC battery input pin is the SD card detect input in this design (high level = card present, polarity inverted by Q24, see 3.12). An RTC battery shall not be connected to this pin
77	+5V (5V_IN_1)	P	VCC5V0_SYSIN	Main power input +5 V (six pins paralleled, see Note 5; permissible voltage range see 4.3.2)
78	GPIO_VREF	I	△ VRTC (OR-ed with the module-internal RTC supply via D2 BAS70-05Q)	Multiplexed: on the CM120 this pin no longer serves as the GPIO level reference (fundamentally different from CM5, see Note 6); it serves as the RTC backup power input via the OR-ing diode; voltage range TBD (see 4.3.2)
79	+5V (5V_IN_2)	P	VCC5V0_SYSIN	Main power input +5 V
80	SCL0	I/O	I2C7_SCL_M2_CAM1 (SoC GPIO3_D2)	Camera/display I ² C clock (corresponds to CM5 SCL0 function); on-board R95381 pull-up to 3.3 V
81	+5V (5V_IN_3)	P	VCC5V0_SYSIN	Main power input +5 V
82	SDA0	I/O	I2C7_SDA_M2_CAM1 (SoC GPIO3_D3)	Camera/display I ² C data; on-board R95382 pull-up to 3.3 V
83	+5V (5V_IN_4)	P	VCC5V0_SYSIN	Main power input +5 V
84	CM5_3.3V (3V3_O_1)	P	VCC_3V3_S0	3.3 V power output (±5%); load capability per pin TBD , see 4.3.2
85	+5V (5V_IN_5)	P	VCC5V0_SYSIN	Main power input +5 V
86	CM5_3.3V (3V3_O_2)	P	VCC_3V3_S0	3.3 V power output (±5%)
87	+5V (5V_IN_6)	P	VCC5V0_SYSIN	Main power input +5 V
88	CM5_1.8V (1V8_O_1)	P	VCC_1V8	1.8 V power output (±5%); load capability per pin TBD
89	WL_nDisable	O	△ MIPI_DPHY_CSI_CAM2_RST_3V3 (SoC GPIO1_B3)	Multiplexed: the CM5 wireless disable pin is the CAM2 camera reset output (3.3 V) in this design. GPIO1 bank, see Note 4
90	CM5_1.8V (1V8_O_2)	P	VCC_1V8	1.8 V power output (±5%)
91	BT_nDisable	O	△ MIPI_CSI_CAM2_CLKOUT_3V3 (level-shifted via U6 at SoC side, output via R26)	Multiplexed: the CM5 Bluetooth disable pin is the CAM2 camera MCLK output (3.3 V) in this design
92	PWR_Button	I	PMIC_RESET_L → RK806 RESETB (U2200-40)	Reset request input / PMIC reset output (corresponds to CM5 PWR_BUT function; connected to the PMIC reset pin, see 3.14 and Chapter 6)
93	nRPIBOOT	I	SARADC_VIN0_BOOT (divider/filter network R9202/R1501/R1502 + C1500; recovery pushbutton SW1)	Boot mode selection input: determined by SARADC analog sampling (threshold TBD , see 3.16); controlled by carrier-board pushbutton or level, see Note 7
94	CC1	I	SARADC_VIN3_3V3 (via R3)	USB-C CC1 analog detect input (for sampling the CC voltage of the USB-C interface connected on the carrier side, see 3.5)
95	LED_nPWR	O	LED_RED_EN (driven directly by SoC GPIO0_C4)	Active-low power indicator LED drive output (corresponds to CM5 LED_nPWR function)
96	CC2	I	SARADC_VIN4_3V3 (via R1)	USB-C CC2 analog detect input (same as pin 94, the other CC line)
97	CAM_GPIO0	O	△ MIPI_DPHY_CSI_CAM1_RST_3V3 (SoC GPIO1_B2)	Multiplexed: CAM1 camera reset output (3.3 V). GPIO1 bank, see Note 4
98	GND	—	GND	Ground (0 V)

Pin	Signal Name (CM5-Compatible)	Dir.	CM120 Actual Function (Net)	Description
99	PMIC_Enable	I	PWRON_L → RK806 PWRON (U2200-4)	PMIC enable / power on-off control input (corresponds to CM5 PMIC_Enable function; timing and polarity definitions see Chapter 6)
100	CAM_GPIO1	O	△ USB_HUB_RST_3V3 (SoC GPIO4_B0)	Multiplexed: the CM5 camera GPIO is the USB Hub reset output (3.3 V, for the carrier-side Hub) in this design

5.2 Pin Definitions (Pins 101–200, Second Connector)

Table 52: Pin definitions (pins 101–200, second connector)

Pin	Signal Name (CM5-Compatible)	Dir.	CM120 Actual Function (Net)	Description
101	USB_OTG_ID	—	NC (single-node net, floating)	OTG ID detection is not used in this design; the OTG role is determined by CC detection (pins 94/96), see 3.5
102	PCle_CLK_nREQ	I	PCIE20X1_2_CLKREQN_M0 (SoC GPIO3_C7)	PCle Channel B clock request (CLKREQ#, active low) input
103	USB_N	I/O	USB20_OTG_DM (SoC ball AY10)	USB2.0 OTG D– (shared with the USB3 OTG port, see 3.5/3.6)
104	PCle_nWAKE	I/O	△ SSTX2P/D3P (SoC ball BB14)	Multiplexed: USB3.1 OTG / DP Alt Mode lane 3 differential positive (Type-C SSTX2 position, see 3.5)
105	USB_P	I/O	USB20_OTG_DP (SoC ball AY11)	USB2.0 OTG D+
106	PCle_PWR_EN	I/O	△ SSTX2N/D3N (SoC ball BA14)	Multiplexed: USB3.1 OTG / DP Alt Mode lane 3 differential negative
107	GND	—	GND	Ground (0 V)
108	GND	—	GND	Ground (0 V)
109	PCle_nRST	O	PCIE20X1_2_PERSTN_M0 (SoC GPIO3_D1)	PCle Channel B reset output (PERST#, active low)
110	PCle_CLK_P	O	PCIE20_0_REFCLKP (SoC ball L42)	PCle Channel A reference clock positive output (frequency TBD, see 3.4)
111	VBUS_EN	I	△ PCIE20X1_2_WAKEN_M0 (SoC GPIO3_D0)	Multiplexed: PCle Channel B wake (WAKE#) input
112	PCle_CLK_N	O	PCIE20_0_REFCLKN (SoC ball K41)	PCle Channel A reference clock negative output
113	GND	—	GND	Ground (0 V)
114	GND	—	GND	Ground (0 V)
115	MIPI0_D0_N	I	MIPI_DPHY0_RX_D0N (SoC ball BB38)	CAM1 camera CSI data 0 negative (MIPI D-PHY RX, 2-lane/4-lane, see 3.11)
116	PCle_RX_P	I	PCIE20_0_RXP (SoC ball J42)	PCle Channel A receive positive; no AC coupling capacitor on module, to be provided on the carrier board (see Note 8)
117	MIPI0_D0_P	I	MIPI_DPHY0_RX_D0P (SoC ball BA38)	CAM1 CSI data 0 positive
118	PCle_RX_N	I	PCIE20_0_RXN (SoC ball J41)	PCle Channel A receive negative; same as pin 116, Note 8
119	GND	—	GND	Ground (0 V)
120	GND	—	GND	Ground (0 V)
121	MIPI0_D1_N	I	MIPI_DPHY0_RX_D1N (SoC ball AY40)	CAM1 CSI data 1 negative
122	PCle_TX_P	O	PCIE20_0_TXP (SoC ball H41)	PCle Channel A transmit positive; no AC coupling capacitor on module, to be provided on the carrier board (see Note 8)
123	MIPI0_D1_P	I	MIPI_DPHY0_RX_D1P (SoC ball BA40)	CAM1 CSI data 1 positive
124	PCle_TX_N	O	PCIE20_0_TXN (SoC ball H42)	PCle Channel A transmit negative; same as pin 122, Note 8
125	GND	—	GND	Ground (0 V)
126	GND	—	GND	Ground (0 V)
127	MIPI0_C_N	I	MIPI_DPHY0_RX_CLKN (SoC ball BA41)	CAM1 CSI clock negative
128	USB3-0-RX_N	I	△ MIPI_CSI0_RX_D0N (SoC ball AL41)	Multiplexed: CAM2 camera CSI data 0 negative (2-lane, see 3.11)
129	MIPI0_C_P	I	MIPI_DPHY0_RX_CLKP (SoC ball BB41)	CAM1 CSI clock positive
130	USB3-0-RX_P	I	△ MIPI_CSI0_RX_D0P (SoC ball AL42)	Multiplexed: CAM2 CSI data 0 positive
131	GND	—	GND	Ground (0 V)
132	GND	—	GND	Ground (0 V)
133	MIPI0_D2_N	I	MIPI_DPHY0_RX_D2N (SoC ball BA42)	CAM1 CSI data 2 negative
134	USB3-0-D_P	I	△ MIPI_CSI0_RX_D1N (SoC ball AK42)	Multiplexed: CAM2 CSI data 1 negative . △ Carrier-board routing shall follow the actual polarity in this table; polarity shall not be inferred from the pin name suffix _P/_N (see Note 9)

Pin	Signal Name (CM5-Compatible)	Dir.	CM120 Actual Function (Net)	Description
135	MIPI0_D2_P	I	MIPLDPHY0_RX_D2P (SoC ball AY42)	CAM1 CSI data 2 positive
136	USB3-0-D_N	I	△ MIPI_CSIO_RX_D1P (SoC ball AK41)	Multiplexed: CAM2 CSI data 1 positive (polarity opposite to the pin name suffix, see Note 9)
137	GND	—	GND	Ground (0 V)
138	GND	—	GND	Ground (0 V)
139	MIPI0_D3_N	I	MIPLDPHY0_RX_D3N (SoC ball AW42)	CAM1 CSI data 3 negative
140	USB3-0-TX_N	I	△ MIPI_CSIO_RX_CLK0N (SoC ball AN41)	Multiplexed: CAM2 CSI clock negative
141	MIPI0_D3_P	I	MIPLDPHY0_RX_D3P (SoC ball AW41)	CAM1 CSI data 3 positive
142	USB3-0-TX_P	I	△ MIPI_CSIO_RX_CLK0P (SoC ball AN42)	Multiplexed: CAM2 CSI clock positive
143	HDMI1_HOTPLUG	O	△ MIPLDPHY_CSI_CAM2_PDN_3V3 (SoC GPIO4_B3)	Multiplexed: the CM5 HDMI1 hot-plug pin is the CAM2 Power-Down control output (3.3 V) in this design
144	GND	—	GND	Ground (0 V)
145	HDMI1_SDA	—	NC	Not connected (HDMI1 has been multiplexed as USB3.1 OTG/DP; this module has no second HDMI)
146	HDMI1_TX2_P	I/O	△ SSRX2P/D2P (SoC ball BB13)	Multiplexed: USB3.1 OTG SuperSpeed / DP Alt Mode lane 2 positive (Type-C SSRX2 position)
147	HDMI1_SCL	—	NC	Not connected
148	HDMI1_TX2_N	I/O	△ SSRX2N/D2N (SoC ball BA13)	USB3.1 OTG / DP lane 2 negative
149	HDMI1_CEC	—	NC	Not connected
150	GND	—	GND	Ground (0 V)
151	HDMI0_CEC	I	HDMI_TX0_CEC_PORT (via RC network, see 3.9)	HDMI0 CEC consumer electronics control input
152	HDMI1_TX1_P	I/O	△ SSTX1P/D1P (SoC ball BB11)	Multiplexed: USB3.1 OTG SuperSpeed TX / DP lane 1 positive (Type-C SSTX1 position)
153	HDMI0_HOTPLUG	I	HDMI_TX0_HPD_PORT (via R95608)	HDMI0 hot-plug detect input (5 V tolerant, may be connected directly to the HDMI connector HPD)
154	HDMI1_TX1_N	I/O	△ SSTX1N/D1N (SoC ball BA11)	USB3.1 OTG SuperSpeed TX / DP lane 1 negative
155	GND	—	GND	Ground (0 V)
156	GND	—	GND	Ground (0 V)
157	USB3-1-RX_N	I	△ PCIE20_2_REFCLKP (SoC ball F41)	Multiplexed: PCIe Channel B reference clock positive . △ The pin name suffix does not match the actual polarity; the carrier board shall connect per this table (see Note 9)
158	HDMI1_TX0_P	I	△ SSRX1P/D0P (SoC ball BB10)	Multiplexed: USB3.1 OTG SuperSpeed RX / DP lane 0 positive (Type-C SSRX1 position)
159	USB3-1-RX_P	I	△ PCIE20_2_REFCLKN (SoC ball F42)	Multiplexed: PCIe Channel B reference clock negative (see Note 9)
160	HDMI1_TX0_N	I	△ SSRX1N/D0N (SoC ball BA10)	USB3.1 OTG SuperSpeed RX / DP lane 0 negative
161	GND	—	GND	Ground (0 V)
162	GND	—	GND	Ground (0 V)
163	USB3-1-D_P	I	△ PCIE20_2_RXP (SoC ball D42)	Multiplexed: PCIe Channel B receive positive; no AC coupling capacitor on module, to be provided on the carrier board (see Note 8)
164	HDMI1_CLK_P	I/O	△ TYPEC_AUXP (SoC ball BA8, SBU1/DPO_AUXP; via C4 AC coupling and R9/R11 network)	Multiplexed: USB Type-C DP Alt Mode AUX channel (half-duplex, AC coupling already on module, see 3.5)
165	USB3-1-D_N	I	△ PCIE20_2_RXN (SoC ball C42)	PCIe Channel B receive negative; see Note 8
166	HDMI1_CLK_N	I/O	△ TYPEC_AUXN (SoC ball BB8, SBU2/DPO_AUXN; via C5 AC coupling and R10/R12 network)	USB Type-C AUX channel negative
167	GND	—	GND	Ground (0 V)
168	GND	—	GND	Ground (0 V)
169	USB3-1-TX_N	O	△ PCIE20_2_TXP (SoC ball E41)	Multiplexed: PCIe Channel B transmit positive (polarity opposite to the pin name suffix, see Note 9); no AC coupling capacitor on module, to be provided on the carrier board (see Note 8)
170	HDMI0_TX2_P	O	HDMI_TX0_D2P (SoC ball BB7; via C90593 220 nF AC coupling + R95080 590 Ω network)	HDMI0 TMDS/FRL channel 2 positive (100 Ω differential pair)
171	USB3-1-TX_P	O	△ PCIE20_2_TXN (SoC ball D41)	Multiplexed: PCIe Channel B transmit negative (see Note 9); see Note 8
172	HDMI0_TX2_N	O	HDMI_TX0_D2N (SoC ball BA7; via C90594 AC coupling)	HDMI0 channel 2 negative
173	GND	—	GND	Ground (0 V)
174	GND	—	GND	Ground (0 V)
175	DSI1_D0_N	O	MIPLDPHY1_TX_D0N (SoC ball BA16)	DSI1 display data 0 negative (MIPI D-PHY TX, see 3.10)
176	HDMI0_TX1_P	O	HDMI_TX0_D1P (SoC ball BA5; via C90595 AC coupling)	HDMI0 channel 1 positive

Pin	Signal Name (CM5-Compatible)	Dir.	CM120 Actual Function (Net)	Description
177	DSI1_D0_P	O	MIPI_DPHY1_TX_D0P (SoC ball BB16)	DSI1 display data 0 positive
178	HDMI0_TX1_N	O	HDMI_TX0_D1N (SoC ball BB5; via C90596 AC coupling)	HDMI0 channel 1 negative
179	GND	—	GND	Ground (0 V)
180	GND	—	GND	Ground (0 V)
181	DSI1_D1_N	O	MIPI_DPHY1_TX_D1N (SoC ball BB17)	DSI1 display data 1 negative
182	HDMI0_TX0_P	O	HDMI_TX0_D0P (SoC ball BB4; via C90597 AC coupling)	HDMI0 channel 0 positive
183	DSI1_D1_P	O	MIPI_DPHY1_TX_D1P (SoC ball BA17)	DSI1 display data 1 positive
184	HDMI0_TX0_N	O	HDMI_TX0_D0N (SoC ball BA4; via C90598 AC coupling)	HDMI0 channel 0 negative
185	GND	—	GND	Ground (0 V)
186	GND	—	GND	Ground (0 V)
187	DSI1_C_N	O	MIPI_DPHY1_TX_CLKN (SoC ball BA19)	DSI1 display clock negative
188	HDMI0_CLK_P	O	TBD	Function and circuit definition to be confirmed
189	TBD	TBD	TBD	Pin definition to be confirmed
190	TBD	TBD	TBD	Pin definition to be confirmed
191	TBD	TBD	TBD	Pin definition to be confirmed
192	TBD	TBD	TBD	Pin definition to be confirmed
193	TBD	TBD	TBD	Pin definition to be confirmed
194	TBD	TBD	TBD	Pin definition to be confirmed
195	TBD	TBD	TBD	Pin definition to be confirmed
196	TBD	TBD	TBD	Pin definition to be confirmed
197	TBD	TBD	TBD	Pin definition to be confirmed
198	TBD	TBD	TBD	Pin definition to be confirmed
199	TBD	TBD	TBD	Pin definition to be confirmed
200	TBD	TBD	TBD	Pin definition to be confirmed

Pending pinout details: the function of pin 188, pin definitions 189–200, and pinout Notes 1–9 are **TBD**.

6 Power

6.1 Power Architecture Overview

6.1.1 Power Input

The CM120 uses a **single +5 V power input**, consistent with the CM5 form factor. +5V is fed into the module through **six paralleled connector pins** (77/79/81/83/85/87, net VCC5V0_SYSIN) (allocation per Chapter 5).

Item	Value	Remarks
Input power	Single +5 V (6 pins paralleled)	
Input voltage (recommended operating condition)	4.75 V ~ 5.25 V (nominal 5.0 V)	Consistent with CM5 (CM5 DS RP-008180-DS-7: 4.75 ~ 5.25 V); within the window of JW5265 input range 2.5 ~ 6 V and RK806 UVLO 2.7 V / OVLO 6.0 V
Input voltage (absolute maximum rating)	-0.3 V ~ +7.0 V	JW5265 DS (PVIN/SVIN -0.3 ~ 7 V); >6.0 V triggers RK806 OVLO protective shutdown (see 6.7); stress rating only, not an operating condition
Input current limit (connector rating)	≤ 1.8 A (6 × 0.3 A / pin, approx. 9 W at 5 V)	DF40C-100DP-0.4V datasheet (see 4.1.3); the carrier-board +5V supply capability shall not be lower than the module power demand and shall in no case be designed to exceed the connector rating
Input current (standby/typical/peak)	TBD	Subject to system-level measurement (see 6.4)
Power-up monotonicity/hold requirement	+5V shall rise monotonically to ≥ 4.75 V and remain ≥ 4.75 V during operation	Per CM5 DS v7 power-up conditions; the CM120 determines input validity through two thresholds: JW5265 UVLO (2.4 V typ) and RK806 VB_OK (2.8 V typ)

Carrier-board constraint (back-feed prevention): Same as for CM5, **no power shall be applied to any module pin before +5V is up** — including back-feeding via 3V3_O/1V8_O and high-level driving of digital pins such as GPIO/Ethernet. Otherwise, unintended supply paths may form through level shifters, load-switch body diodes,

etc., causing power-up sequence disorder or device damage. Carrier boards with multiple supplies shall be checked path by path (**TBD**, per-path analysis).

6.1.2 Power Tree

1	+5V (connector 77/79/81/83/85/87, VCC5V0_SYSIN)
2	D5 (B5819WS Schottky) → HDMI_5V (HDMI DDC/CEC 5V domain, see \ref{cm120-section-5-6-7})
3	U2 JW5265 (pre-regulator buck, always enabled) - L1 1.5μH/5A → VCC_SYSIN (4.04 V, design value)
4	U2200 RK806-1 (PMIC): -BUCK110 + -NLD015 + -PLD016 (see \ref{cm120-section-5-5-2})
5	EXT_EN -R2305 10Ω → U8 EN
6	U2300 RK860 - L2300 → VDD_CPU_BIG0_S0
7	U2301 RK860 - L2301 → VDD_CPU_BIG1_S0 -FB2300 → bead VDD_CPU_BIG1_MEM_S0
8	U2302 RK860 - L2302 → VDD_NPU_S0 (all three share BIG/NPU_EN; I2C voltage scaling see \ref{cm120-section-5-6-6})
9	U8 SY8089AAAC - L2303 2.2μH → VCC_1V1_NLD0_S3 (1.1V)
10	Inputs of RK806 -NLD015 (VCC13/VCC14)
11	
12	VCC_3V3_S3 (BUCK8) - U3 SGM2590D load switch → VCC_3V3_S0 → 3V3_0 pins (84/86)
13	VCC_1V8_S0 (PLD02) - R40 0Ω → VCC_1V8 → 1V8_0 pins (88/90)
14	VRTC (pin 78) ⊕ VCC_3V3_S3 - D2 (BAS70-05Q) → VCC_RTC → U1 HYM8563TS (RTC)

6.1.3 Pre-Regulator Buck (U2 JW5265 → VCC_SYSIN)

+5V is first stepped down by U2 to the **module main distribution voltage VCC_SYSIN**, which then serves as the input to all RK806 BUCKs, the three RK860s, and U8.

Item	Value
Device	JW5265 (DFN3×3-10; JW5265/JW5265F DS Rev 0.8)
Enable scheme	Always enabled: EN pulled up to VCC5V0_SYSIN via R16 (100 kΩ) (EN rising threshold 1.2 V typ / 1.35 V max)
Input range	2.5 ~ 6 V; UVLO 2.4 V (typ, rising) / 200 mV hysteresis
Output voltage VCC_SYSIN	4.04 V (design value)
Output inductor	L1 = 1.5 μH / 5 A
Maximum output current	5 A continuous; PFET current limit 7.8 A (typ, 6.5 ~ 9.4 A)
Switching frequency / control	1 MHz (typ), COT control; PFM at light load (JW5265)
Quiescent / shutdown current	Iq = 60 μA (typ) / 90 μA (max); Isdn = 0.1 μA (typ) / 1 μA (max)

Item	Value
Soft-start / protection	Soft-start 0.65 ms (typ, without CSS); output discharge 40 Ω ; hiccup short-circuit protection; TSD 150 °C (20 °C hysteresis)
Downstream loads	RK806 VCC1–12 + VCCA (via R95029 0 Ω), 3×RK860, U8

Design implication: VCC_SYSIN is an **always-on rail** (present whenever +5V is present, independent of PMIC on/off state). With the PMIC shut down, the module input quiescent current still includes the JW5265 quiescent current (60 μ A typ, see 6.4.2). The connection of the PG pin (open-drain power-good indication) on the module is **TBD** (not used in the parsed netlist; separate confirmation is required if intended for carrier-board sequencing).

6.1.4 Power Management Device Summary

Ref.	Device	Role	Key Parameters (per respective datasheets)	Configuration Interface
U2	JW5265	Pre-regulator buck → VCC_SYSIN	Input 2.5–6 V, output 5 A, VFB 0.6 V, 1 MHz, Iq 60 μ A / Isdn 0.1 μ A, UVLO 2.4 V, current limit 7.8 A typ, TSD 150 °C	FB resistor fixed (R18/R21 → 4.04 V), always enabled
U2200	RK806-1 PMIC (QFN68)	10×BUCK + 5×NLDO + 5×PLDO + VCCIO LDO	UVLO 2.7 V / OVLO 6.0 V / TSD 140 °C / VB_OK 2.8 V (typical)	SPI (R2258 100 k Ω pull-down on CS selects SPI mode)
U2300/2301/2302	RK860 ×3	CPU BigCore0/BigCore1/NPU core supplies	2.4 MHz, 7 A continuous / 8.5 A peak; 0.5–1.5 V, 6.25 mV steps (class 0xA), default 0.8 V; UVLO 2.55 V, OVP 6 V, TSD 150 °C	I2C + VSEL (see 6.6.6)
U3	SGM2590D	3.3 V load switch	Current limit set by R33 (4.3 k Ω , OCB), limit value TBD	EN level (divided from PLDO2)
U8	SY8089AAAC	Auxiliary buck → 1.1 V (NLDO input)	≈1.1 V (R2306 100 k Ω / R2307 120 k Ω , derived with VFB = 0.6 V, consistent with net name VCC_1V1_NLDO_S3); current capability TBD	EN = RK806 EXT_EN (via R2305 10 k Ω)
U1	HYM8563TS	RTC	Supplied by VCC_RTC; backup current TBD	I2C2_M0
D2	BAS70-05Q	RTC supply OR-ing	Schottky ORing	—
D5 / D2600	B5819WS	HDMI 5V generation / VDC negative clamp	—	—

The RK860 version (RK860-2/-3, i.e., class 0xA 0.5–1.5 V) is inferred from the RK3588S core voltage domain range (0.55–1.05 V) and I2C address uniqueness on the shared bus (U2300/U2301 share I2C0 and shall use the two addresses 0x42/0x43); **the exact model and addresses are subject to the BOM.**

6.2 Power-up Sequencing

6.2.1 Power-up Preconditions

1. **+5V input:** via pins 77–87, JW5265 establishes the always-on voltage VCC_SYSIN (4.04 V, design value); +5V shall rise monotonically to ≥ 4.75 V and hold (see 6.1.1 and 4.3.2).
2. **No pin feed before power-up:** see the carrier-board constraint in 5.1.1.
3. **EEPROM write protection:** if write protection of the on-board EEPROM is required, EEPROM_NWP (pin 20) shall be held low before +5V power-up (see 3.17 and Chapter 5).
4. **Boot mode:** if special boot modes such as USB/Maskrom are required, the associated mode pins shall be held at valid levels before the SoC reset is released.

6.2.2 Power-on Trigger Methods

After VCCA/VCC1/VCC2 rises above **VB_OK** (typical 2.8 V, i.e., the VCC_SYSIN domain), the RK806-1 supports three power-on methods (RK806 manual Section 4.1.2). The CM120 actually uses the first two:

Trigger Method	CM120 Implementation	Behavior
① VDC high level (default automatic power-on)	Module-internal VDC RC trigger circuit (6.6.4): at the moment VCC_SYSIN powers up, a ≈ 2 V pulse is generated at the VDC pin, far exceeding the 0.88 V threshold and lasting far longer than 2 ms	The module powers on automatically after +5V is applied , no carrier-board intervention required
② PWRON key	PMIC_ENABLE (pin 99) pulled low for ≥ 20 ms (default debounce, register-programmable to 500 ms)	After software shutdown, the carrier board may pull pin 99 low for ≥ 20 ms to power on again; or re-apply +5V (VDC re-triggers)
③ ABNORMAL ON	Automatic restart after OVP/UVLO when register 0x5F<7>=0	Protective recovery, not a normal design state

⚠ **Key difference from CM5:** CM5 requires a “PMIC_EN rising” as a necessary power-on condition (floating/low level does not power on); **on the CM120, the module still powers on automatically with +5V even when pin 99 is left floating** (internal VDC trigger). PMIC_ENABLE on the CM120 is a **power key / shutdown control input** rather than a necessary power-on condition. Applications requiring “pushbutton/controlled power-on” shall manage +5V switching on the carrier-board side (eFuse/load switch),

noting that the floating level of pin 99 is set by the RK806 internal $\sim 45\text{ k}\Omega$ pull-up to VCCA ($\approx 4\text{ V}$, derived).

After software shutdown (Method ② in 6.3.2), VCC_SYSIN remains present, but the VDC pulse has decayed to zero (capacitor DC blocking), so the PMIC **remains off and does not repeatedly power on by itself** — until PMIC_ENABLE is pulled low for $\geq 20\text{ ms}$ or +5V is re-applied. This behavior is compatible with the CM5 semantics of “pulling PMIC_EN low to enter the lowest power mode”.

6.2.3 RK806-1 Power-up Sequencing (Main PMIC)

Once triggered, all PMIC channels power up sequentially at **1 ms intervals** in the fixed sequence preset by factory OTP (RK806-1 manual Table 4-1; the OTP version of the CM120 is **TBD**). The correspondence between channels and CM120 power rails:

Seq. No.	RK806-1 Channel	CM120 Power Rail	Default Voltage	Capability	Main Load Domains
1	BUCK7	VCC_2V0_PLDO_S3	2.0 V	3 A	PLDO1/2/3 inputs (VCC11), SD card detect pull-up (R95605)
2	BUCK3	VDD_LOGIC_S0	0.75 V	5 A	SoC core logic
2	BUCK5	VDD_DDR_S0	0.85 V	3 A	SoC DDR controller logic and MIF
2	NLDO1-5	VDD_0V75_S3 / VDDA_DDR_PLL_S0 / VDDA_0V75_S0 / VDDA_0V85_S0 / HDMI_VDDA0V85_S0	0.75/0.85/0.75/0.85/0.75 V	300/300/500/500/300 mA	SoC PMU, DDR PLL, MIPI/USB/OTP/PLL analog, Combo PIPE PHY, HDMI/eDP TX0 analog (NLDO input see 6.2.4 △)
3	BUCK2	VDD_CPU_LIT_S0	0.75 V	5 A	SoC CPU Little cores + MEM balls
3	BUCK10	VCC_1V8_S3	1.8 V	3 A	eMMC VCCQ/VCCIO_FLASH (R4000), PMU IO domains (R2211→VCC1V8_PMU_DDR_S3, also LPDDR4 VDD1), INT/RESETB pull-ups, 1V8_O alternative position (R39 NC)
3	PLDO1/2/6	VCCA_1V8_S0 / VCC_1V8_S0 / VCCIO (PLDO6)	1.8 V×3	500/300/300 mA	SoC all AVDD1V8; VCCIO1/2/4/5/6 1V8 balls + 1V8_O (R40) ; PLDO6 for PMIC interface self-use
4	BUCK6	VDD2_DDR_S3	1.1 V (external feedback, derived)	3 A	LPDDR4 ×2 VDD2
4	PLDO3	VDDA_1V2_S0	1.2 V	300 mA	SoC MIPI D/C PHY VDD 1.2 V
5	BUCK1	VDD_GPU_S0	0.75 V	6.5 A	SoC GPU core + GPU_MEM balls
5	BUCK4	VDD_VDENC_S0	0.75 V	5 A	SoC VCODEC + MEM balls
6	BUCK8	VCC_3V3_S3	3.3 V	3 A	eMMC VCC, PMUIO2 3V3 balls, U3 input (→3V3_O), RTC OR-ing (D2.A2), I2C pull-ups, RK860 EN divider
6	BUCK9	VDDQ_DDR_S0	0.6 V (external feedback, derived)	3 A	SoC DDR VDDQ, LPDDR4 VDDQ (via R3808)
6	PLDO4/5	VCCA_3V3_S0 / VCCIO_SD_S0	3.3 V×2	500/300 mA	SoC USB20 AVDD33; SoC VCCIO2 (SD IO) 3V3 balls
11	RESETB	PMIC_RESET_L released	—	—	SoC reset released (see 6.2.7)

Notes:

- Inter-channel delay is 1 ms; a margin of $\geq 5\text{ ms}$ is reserved after Seq. 6 until RESETB (Seq. 11) (per RK806-1 sequence definition, **TBD** for measurement confirmation).
- Power-up default voltages are the RK806-1 factory defaults; after system boot, the SoC reconfigures each rail voltage via PMIC_SPI (**TBD**, power design calculations / PMIC firmware).

- **BUCK6/BUCK9 external feedback dividers** (supported on BUCK1/2/5/6/9, $V_{ref_exfb} = 0.5\text{ V}$, enabled via registers 0xFD/0xFE):
 - BUCK6: $R_{2218}\ 120\text{ k}\Omega + R_{2227}\ 100\text{ k}\Omega \rightarrow \mathbf{1.1\text{ V}}$ = LPDDR4 VDD2 nominal;
 - BUCK9: $R_{2236}\ 20\text{ k}\Omega + R_{2241}\ 100\text{ k}\Omega \rightarrow \mathbf{0.60\text{ V}}$ = LPDDR4 VDDQ nominal.
 - If the exfb enable bit is not preset by OTP, the output at power-up moment is the internal-feedback default 0.5 V, switching after SoC configuration (actual behavior depends on OTP/firmware).
- **LPDDR4 power-up order verification:** VDD1 (1.8 V, Seq. 3) $\rightarrow$ VDD2 (1.1 V, Seq. 4) $\rightarrow$ VDDQ (0.6 V, Seq. 6), satisfying the LPDDR4 requirement that “VDD1 and VDD2 precede VDDQ”.

6.2.4 EXT_EN Auxiliary Power Chain (VCC_1V1_NLDO_S3)

During the RK806-1 power-up process, **EXT_EN** is output (relative timing $T1 = 3.5\sim 100\text{ ms}$ per the manual figure, used to validate external supply readiness; this pin also serves as master/slave selection — this design uses a single PMIC, so it functions as EXT_EN). It enables **U8 (SY8089AAAC)** via R2305 (10 k Ω), generating **VCC_1V1_NLDO_S3 ($\approx 1.1\text{ V}$)** from VCC_SYSIN as the **input supply for all RK806 NLDOs (VCC13/VCC14)**.

6.2.5 RK860 Big-Core/NPU Supplies

The three RK860s share the enable signal **BIG/NPU_EN**: R2302 (100 k Ω) pulled up to VCC_3V3_S3 + R2303 (120 k Ω) pulled down to GND, dividing to $\approx 1.8\text{ V} > \text{EN } V_{IH}$ (1.1 V). Therefore:

1. Once VCC_3V3_S3 (BUCK8, Seq. 6) is established, the three RK860s are **automatically enabled** without SoC intervention;
2. The power-up default output is the VSEL0/VSEL1 register reset value **0.8 V** (both register sets have identical reset values, no risk from the initial VSEL pin state); typical soft-start 260 μs ;
3. After SoC boot, voltages are adjusted online per the DVFS policy via **I2C0_M2** (U2300/U2301) and **I2C2_M0** (U2302) (0.5–1.5 V, 6.25 mV steps);
4. The VSEL pins connect to SoC GPIOs respectively (VSEL2 $\rightarrow$ GPIO0_A3_D, VSEL6 $\rightarrow$ GPIO0_D6_D, VSEL3 $\rightarrow$ GPIO0_C1_D) for fast switching between the two register sets;
5. VDD_CPU_BIG1_S0 additionally derives VDD_CPU_BIG1_MEM_S0 through the **FB2300 bead** (see 6.5.2).

6.2.6 External Output Rails (3V3_O / 1V8_O) Power-up Order $\triangle$ Opposite to CM5

Output Rail	Source	Power-up Time	Remarks
1V8_O (88/90)	PLDO2 (Seq. 3) via R40 (0Ω, populated)	Seq. 3 (approx. 3rd ms)	R39 (NC/0 Ω , from VCC_1V8_S3) is an alternative bridge position, not populated
3V3_O (84/86)	BUCK8 (Seq. 6) via U3 (SGM2590D) load switch	Seq. 6 (approx. 6th ms)	U3's EN divides ≈ 1.6 V via R32 10 k Ω (from PLDO2) / R31 100 k Ω — once PLDO2 is ready, U3 is already enabled, and its output follows its input VCC_3V3_S3

$\triangle$ **On the CM120, 1V8_O powers up before 3V3_O** (Seq. 3 vs Seq. 6, approx. 3 ms apart). **This is opposite to CM5** (CM5: +3.3V first, +1.8V at least 1 ms later). Carrier-board circuits directly reused from CM5 designs that are sensitive to the order of these two rails (power-on reset strategy, dual-rail device power-up order requirements) **must be reviewed** when ported to the CM120.

6.2.7 Power-up Sequence Summary

1. **+5V applied** $\rightarrow$ JW5265 (always enabled) soft-start (0.65 ms typ) $\rightarrow$ **VCC_SYSIN (4.04 V)** established;
2. RK806 VCCA/VCC crosses **VB_OK** (typical 2.8 V) $\rightarrow$ power-on conditions met (input validity check window $T_1 = 3.5\sim 100$ ms);
3. **VDC RC trigger** (module-internal, 6.6.4) or **PMIC_ENABLE pulled low for ≥ 20 ms** $\rightarrow$ PMIC powers on;
4. RK806-1 channels power up step by step at **1 ms intervals**: Seq. 1 (2.0 V) $\rightarrow$ Seq. 2 (logic/DDR logic + NLDO domains) $\rightarrow$ Seq. 3 (CPU Little cores, 1.8 V domains, PLDO1/2/6) $\rightarrow$ Seq. 4 (LPDDR4 VDD2 1.1 V, 1.2 V) $\rightarrow$ Seq. 5 (GPU, VDENC) $\rightarrow$ Seq. 6 (3.3 V domains, LPDDR4 VDDQ 0.6 V); (NLDO actual readiness is constrained by 6.2.4)
5. **EXT_EN output** $\rightarrow$ U8 enabled $\rightarrow$ **VCC_1V1_NLDO_S3 (1.1 V)** established $\rightarrow$ NLDO1–5 ready;
6. **RK860 $\times 3$ automatically enabled with VCC_3V3_S3 (Seq. 6)**, big-core/NPU rails output at default 0.8 V;
7. Seq. 11: **RESETB driven high** $\rightarrow$ SoC NPOR released $\rightarrow$ SoC boots, reconfiguring supplies and DVFS via PMIC_SPI / I2C0 / I2C2;
8. **3V3_O/1V8_O** supply the carrier board at Seq. 6/Seq. 3 respectively (order see 6.2.6 $\triangle$).

6.3 Power-down Sequencing

6.3.1 Normal Shutdown Procedure

Following the CM5 recommended procedure: **the operating system shall first perform a software shutdown (shutdown/poweroff)** to ensure file system consistency; where this cannot be guaranteed, the carrier board should consider a read-only file system or an overlay scheme (btrfs/f2fs/overlayfs, etc.).

After the OS shutdown completes, the CM120 has two paths to enter the lowest power state:

Path	Operation	Effect	CM5 Counterpart
① Disconnect +5V	Remove the +5V input	The entire module (including VCC_SYSIN and the RTC main backup source) loses power	CM5 "remove the +5V rail"
② Software shutdown (recommended)	At OS shutdown, write register 0x72<0>=1 via PMIC_SPI (see Method ② in 6.3.2)	The PMIC shuts down all channels in the 6.3.3 order; VCC_SYSIN remains present (JW5265 always enabled), and the RTC continues to be maintained by the carrier-board VRTC (pin 78)	≈ CM5 "pull PMIC_EN low" lowest-power mode, but the mechanism differs (see below)

6.3.2 Shutdown Trigger Methods (RK806-1: 7 Methods)

The following methods (unless otherwise noted) all trigger the **same power-down sequence (6.3.3)**. The only CM120-relevant hardware pin is PWRON (= PMIC_ENABLE pin 99); PWRCTRL/SYNC are not routed to the connector (**verification**: not found connected to the BTB in the netlist, TBD for confirmation).

#	Method	Trigger Conditions (RK806-1 Manual 4.1.3)	CM120 Availability
①	Long-press PWRON	In ON/SLEEP state, 0x76<6>=0, PWRON held low for 6/8/10/12 s (duration I2C/SPI programmable)	Carrier board pulls pin 99 low and holds
②	Write shutdown register	Write 0x72<0>=1 in ON/SLEEP state	Software shutdown (normal OS shutdown path)
③	SYNC pulled low	When 0x5F<7>=1 and VCCA/VCC1/VCC2 crosses the UV (2.7 V) / OV (6.0 V) thresholds, SYNC immediately goes low and the PMIC shuts down immediately	Single-PMIC design, SYNC not connected externally (TBD net verification)
④	Input undervoltage VB_LO	0x5E<3>=0 and VCCA/VCC1/VCC2 < 3.2 V for 1 ms	Protective shutdown upon +5V/VCC_SYSIN collapse
⑤	PWRCTRL pin	PWRCTRLn_FUN=010 and PWRCTRLn asserted (polarity programmable)	Depends on SoC GPIO routing (TBD)
⑥	Over-temperature TSD	Die temperature > 140 °C (typical)	Protective, see 6.7

#	Method	Trigger Conditions (RK806-1 Manual 4.1.3)	CM120 Availability
②	ABNORMAL	0x5F<7>=0 and input crosses UV/OV thresholds	Protective (when 0x5F<7>=1, changed to SYNC-low, i.e., Method ③)

The **default debounce duration and OTP configuration of the long-press in Method ① are TBD**; if 0x76<6>=1 during the long press, it becomes a **reset (6.3.4)** instead of a shutdown.

6.3.3 Power-down Order

When the PMIC shuts down (RK806-1 manual Fig. 4-4):

1. **RESETB immediately driven low** → SoC NPOR asserted; the processor enters reset before the power rails collapse;
2. After a 1 ms debounce, **all power channels shut down one by one in the order set by the power-down sequence registers (0xB2~0xC3)** (by default corresponding to the power-up sequence, 1 ms channel spacing, approximately 6 ms for the full chain; actual order subject to OTP/software configuration, **TBD**);
3. Each BUCK/NLDO/PLDO output is discharged internally (**discharge time depends on output capacitance, TBD for measurement**);
4. **EXT_EN de-asserted** → U8 shuts down → VCC_1V1_NLDO_S3 collapses → NLDO1–5 inputs removed;
5. The RK860 x3 shut down as the BIG/NPU_EN divider voltage (VCC_3V3_S3 disappears) falls below the EN threshold; big-core/NPU rails discharge through the internal 150 Ω (RK860 manual);
6. Ultimately only the following remain: **VCC_SYSIN (always on, 4.04 V)**, **VCC_RTC** via D2 OR-ing (if the carrier board provides VRTC); all external rails such as 3V3_O/1V8_O shall be 0 V.

Power-down order of external output rails:

Output Rail	Shutdown Mechanism	Relative Order
3V3_O	U3 input VCC_3V3_S3 (BUCK8) shuts down	After 1V8_O (if the power-down order mirrors power-up)
1V8_O	PLDO2 shuts down	Before 3V3_O

⚠ **Similarity with CM5:** CM5 explicitly states that “+1.8V discharges before +3.3V at shutdown”; if the CM120 adopts the default power-down order mirroring power-up, it is likewise **1V8_O first, 3V3_O last**. However, the RK806 power-down order can be rearranged via registers 0xB2~0xC3; **the final power-down order is subject to OTP/software configuration (TBD)**. Carrier-board circuits sensitive to power-down order shall be verified by measurement before design freeze.

6.3.4 Reset (Non-Power-down) Behavior

The following methods cause the PMIC to reset the SoC (RESETB output pulse) while **maintaining power channel outputs** (or re-executing the power-up sequence per configuration); they are listed so that carrier-board designs can avoid unintended triggering:

#	Method	Conditions	Behavior
①	Long-press PWRON	0x76<6>=1, long press 6/8/10/12 s	Restart (RESETB reset + power re-up sequence) instead of shutdown
②	PWRCTRLn_FUN=011	PWRCTRLn asserted	Reset
③	RESETB pin pulled low	PWR_BUT (pin 92) pulled low externally	Directly resets the SoC (without removing power); note that the RESETB node already has 0.2 μF of capacitance to ground on the module (C2262+C1110); any additional capacitance on the carrier board shall not bring the total above 0.3 μF (RK806 manual limit) — i.e., the carrier-side margin is only 0.1 μF
④	WDT reset	0x73<4:3>=11	Watchdog reset
⑤	Write reset register	0x72<7:5>=001	Software reset

Semantics of pin 92 (PWR_BUT) vs pin 99 (PMIC_ENABLE): pin 92 = RESETB (re-set request, triggered by pulling the active-high node low); pin 99 = PWRON (power key: short press ≥20 ms for power-on / programmable debounce, long press for shutdown or reset). The carrier-board “RESET” button shall connect to pin 92, and the “Power/ON-OFF” button shall connect to pin 99; **they shall not be interchanged**.

6.3.5 +5V Loss and RTC Survival

When +5V is removed abruptly: VCC_SYSIN collapses through downstream load discharge → the RK806 triggers Method ④ (VB_LO 3.2 V/1 ms) or Method ⑤ to shut down all rails → the module loses power. **Abrupt power loss does not guarantee file system consistency**; the carrier-board application layer shall be handled per the same recommendations as for CM5 (see 6.3.1).

After +5V removal, the supply of the RTC (U1 HYM8563TS) depends on whether the carrier board provides **VRTC (pin 78)**:

Carrier-Board VRTC Status	RTC Behavior after +5V Removal
VRTC provided (e.g., 3 V coin cell)	D2 (BAS70-05Q) automatically switches to the VRTC side and RTC timekeeping is maintained; required VRTC voltage/current specifications per Sections 4.3.1 / 4.3.2 (RTC backup ratings are TBD) and the U1 datasheet
Not provided (pin 78 floating)	VCC_RTC discharges to zero along with VCC_3V3_S3; the RTC loses time

6.4 Power Consumption

6.4.1 Module-Level Power Consumption

The actual power consumption of the CM120 is strongly task-dependent (same as for CM5). Module-level values shall be determined by **system-level measurement**; all values are currently **TBD**:

State	Conditions	Typical	Remarks
Shutdown (after software shutdown, +5V present)	PMIC shut down; JW5265/pre-regulator always-on rail unloaded	TBD	≥ U2 quiescent current + RK806 shutdown current (approx. 10–12 μA class) + U8/U3 etc. quiescent currents
RTC-only (+5V removed, VRTC supplied)	Only U1 supplied via D2	TBD	BAS70-05Q reverse leakage + HYM8563TS backup current
Standby/suspend (SLEEP)	OS suspend	TBD	Depends on 0x0C/0x0D/0x61<1> low-power configurations
Idle (OS idle)	Desktop/system idle	TBD	
Typical operation	Regular load	TBD	
Peak	CPU/GPU/NPU fully loaded	TBD	Constrained by the U2 current capability upper limit

6.4.2 Power Device Quiescent/Shutdown Currents (Chip-Level Reference Values)

The following are datasheet values of each device, for estimating the module floor current (rails unloaded; load currents to be added separately):

Device	Parameter	Value	Conditions
RK806-1	Shutdown current I _{sd}	10–12 μA	Shutdown state (VCC_SYSIN present)

Device	Parameter	Value	Conditions
RK806-1	Operating quiescent Iq1	1.8 mA	ON state
RK806-1	SLEEP state Isleep	0.85 mA	SLEEP state
RK860 ×3	Quiescent current Iq	70 µA/piece (×3 = 210 µA)	EN=H, light load
RK860 ×3	Soft-shutdown current Isd_soft	25 µA/piece	EN=H, BUCK_EN=L
RK860 ×3	Shutdown current Isd	0.1 µA/piece	EN=L
U8 SY8089AAAC	Quiescent/shutdown current	TBD	Datasheet not obtained
U2 JW5265	Quiescent current Iq	60 µA (typ) / 90 µA (max)	JW5265 DS (VEN=5 V, IOUT=0, VFB=0.7 V)
U2 JW5265	Shutdown current Isdn	0.1 µA (typ) / 1 µA (max)	JW5265 DS (VIN=6 V, VEN=0 V; on the CM120, EN is always pulled up and never enters this state, so the actual floor current is at the Iq level)
U3 SGM2590D	Quiescent/shutdown current	TBD	Datasheet not obtained
U1 HYM8563TS	RTC backup current	TBD	Datasheet not obtained

6.4.3 Form-Factor Reference (CM5 Measured Values, Not CM120 Specifications)

For carrier-board power budget reference only, **source: CM5 Datasheet RP-008180-DS-7 (v7)**: CM5 lowest-power mode (PMIC_EN low) typical **1.3 mA**; idle typical **400 mA**; typical operation approximately **900 mA** (all vary substantially with OS and tasks). Due to the different power architecture of the CM120 (always-enabled pre-regulator buck, VDC automatic power-on), **the above values are not directly applicable** and serve as order-of-magnitude reference only.

6.5 Regulator Outputs

6.5.1 Output Rails to the Carrier Board

To facilitate carrier-board design, the module provides two regulated output rails through the connector. **The current capability of the two rails available for external peripherals is TBD** (constrained by BUCK8/PLDO2 capacity and module-internal load allocation; see the margin analysis in the table below); loads external to the carrier board are **not included** in the Section 6.4 module power consumption figures (consistent with the CM5 convention).

Output	Connector Pins	Voltage	Supply Source	Device Capability	Module-Internal Occupancy	Carrier-Usable Margin
3V3_O	84 / 86	3.3 V	BUCK8 (VCC_3V3_S3) via U3 load switch (VCC_3V3_S0)	BUCK8 3 A; U3 current limit TBD (R33=4.3 kΩ)	eMMC VCC, PMUIO2, I2C pull-ups, RTC OR-ing, RK860 EN divider, SD card interface (TBD per-load accounting)	TBD

Output	Connector Pins	Voltage	Supply Source	Device Capability	Module-Internal Occupancy	Carrier-Usable Margin
1V8_O	88 / 90	1.8 V	PLDO2 (VCC_1V8_S0) via R40 0 Ω (VCC_1V8)	PLDO2 300 mA	SoC AVDD1V8 domains, VCCIO 1V8 balls, etc. (TBD per-load accounting)	TBD (strongly constrained by the 300 mA limit; expected to be significantly less than the CM5's 600 mA)

⚠ **Capability difference warning vs CM5:** each of the two CM5 rails is rated at 600 mA for external supply; the CM120's 1V8_O is upstream-limited by PLDO2 (300 mA capability), so **a carrier board that budgets 1.8 V peripherals at the CM5's 600 mA will exceed the CM120's capability**. 3V3_O is likewise constrained by the U3 current limit (TBD). Carrier-board designs shall use the official values once the TBD items are finalized.

⚠ The U3 current limit is set by R33 (4.3 k Ω , OCB pin); **the current-limit threshold is TBD** (SGM2590D datasheet not obtained); the behavior of 3V3_O after over-current triggering (hiccup/latch-off) is **TBD**.

6.5.2 Module-Internal Power Rail Summary

Per the netlist and the RK806-1 default sequence (Tables 67–69), RK860 (Table 70), pre-regulator and auxiliary (Table 71), and external domains (Table 72). Voltage accuracy, ripple, load regulation and other parameters are **TBD** (to be supplemented per RK806/RK860 datasheets and system-level measurement).

Table 67: RK806-1 BUCK Outputs (VCC_SYSIN Input)

Channel	Power Rail	Default Voltage	Capability	Power-up Seq.	Main Loads
BUCK1	VDD_GPU_S0	0.75 V	6.5 A	5	SoC GPU core + GPU_MEM balls
BUCK2	VDD_CPU_LIT_S0	0.75 V	5 A	3	SoC CPU Little cores + MEM balls
BUCK3	VDD_LOGIC_S0	0.75 V	5 A	2	SoC core logic
BUCK4	VDD_VDENC_S0	0.75 V	5 A	5	SoC VCODEC + MEM balls
BUCK5	VDD_DDR_S0	0.85 V	3 A	2	SoC DDR controller logic and MIF
BUCK6	VDD2_DDR_S3	1.1 V (external FB, derived)	3 A	4	LPDDR4 $\times$ 2 VDD2
BUCK7	VCC_2V0_PLDO_S3	2.0 V	3 A	1	PLDO1/2/3 inputs (VCC11), SD card detect pull-up
BUCK8	VCC_3V3_S3	3.3 V	3 A	6	eMMC VCC, PMUIO2, U3 input ($\rightarrow$ 3V3_O), RTC OR-ing, I2C pull-ups, RK860 EN divider
BUCK9	VDDQ_DDR_S0	0.6 V (external FB, derived)	3 A	6	SoC DDR VDDQ, LPDDR4 VDDQ (via R3808)
BUCK10	VCC_1V8_S3	1.8 V	3 A	3	eMMC VCCQ/VCCIO_FLASH, VCC1V8_PMU_DDR_S3 (LPDDR4 VDD1), pull-up domains, R39 alternative position (NC)

Table 68: RK806-1 NLDO Outputs (Input = VCC_1V1_NLDO_S3, via VCC13/VCC14)

Channel	Power Rail	Default Voltage	Capability	Power-up Seq.	Main Loads
NLDO1	VDD_0V75_S3	0.75 V	300 mA	2	SoC PMU domain

Channel	Power Rail	Default Voltage	Capability	Power-up Seq.	Main Loads
NLDO2	VDDA_DDR_PLL_S0	0.85 V	300 mA	2	SoC DDR PLL analog
NLDO3	VDDA_0V75_S0	0.75 V	500 mA	2	SoC MIPI/USB/OTP/PLL analog domains
NLDO4	VDDA_0V85_S0	0.85 V	500 mA	2	SoC Combo PIPE PHY analog
NLDO5	HDMI_VDDA0V85_S0	0.75 V	300 mA	2	SoC HDMI/eDP TX0 analog (rail name inconsistent with default voltage, TBD for OTP verification)

△ The actual readiness time of all NLDOs is constrained by the 6.2.4 EXT_EN→U8 chain; the NLDO input is **1.1 V** (not VCC_SYSIN), so only rails with output voltage ≤1.1 V can be realized by this topology — consistent with the rails in the table above (≤0.85 V).

Table 69: RK806-1 PLDO Outputs (Input = VCC_2V0_PLDO_S3, via VCC11)

Channel	Power Rail	Default Voltage	Capability	Power-up Seq.	Main Loads
PLDO1	VCCA_1V8_S0	1.8 V	500 mA	3	SoC all AVDD1V8 domains
PLDO2	VCC_1V8_S0	1.8 V	300 mA	3	SoC VCCIO 1V8 balls + 1V8_O (via R40)
PLDO3	VDDA_1V2_S0	1.2 V	300 mA	4	SoC MIPI D/C PHY VDD 1.2 V
PLDO4	VCCA_3V3_S0	3.3 V	500 mA	6	SoC USB20 AVDD33
PLDO5	VCCIO_SD_S0	3.3 V	300 mA	6	SoC VCCIO2 (SD IO) 3V3 balls
PLDO6	VCCIO (PMIC self-use)	1.8 V	300 mA	3	RK806 interface level domain

The PLDO input is 2.0 V, so the **output upper limit is <2.0 V** — yet PLDO4/5 are nominally 3.3 V: **their actual input must not be (or must not only be) VCC_2V0_PLDO_S3, TBD (verify VCC12 and the PLDO4/5 supply networks);** the 3.3 V values in the table above are inferred from rail names and load domains.

Table 70: RK860 Outputs (VCC_SYSIN Input)

Ref.	Power Rail	Default Voltage	Capability	Enable	Voltage-Scaling Interface
U2300	VDD_CPU_BIG0_S0	0.8 V (VSEL register reset value)	7 A continuous / 8.5 A peak	BIG/NPU_EN (automatic, see 6.2.5)	I2C0_M2 + VSEL (GPIO0_A3_D)
U2301	VDD_CPU_BIG1_S0 → via FB2300 bead → VDD_CPU_BIG1_MEM_S0	0.8 V	7 A / 8.5 A	BIG/NPU_EN	I2C0_M2 + VSEL (GPIO0_D6_D)
U2302	VDD_NPU_S0	0.8 V	7 A / 8.5 A	BIG/NPU_EN	I2C2_M0 + VSEL (GPIO0_C1_D)

Output range 0.5–1.5 V (6.25 mV steps, class 0xA; **model/addresses subject to BOM, TBD**); adjusted online by SoC DVFS during operation; soft-start 260 μs; discharged via internal 150 Ω at shutdown.

Table 71: Pre-Regulator and Auxiliary Supplies

Power Rail	Voltage	Source	Purpose
VCC_SYSIN	4.04 V (design value, $\pm 2\%$ class)	U2 JW5265 (+5V $\rightarrow$ L1 1.5 μ H, VFB 0.6 V $\times$ R18 47 k Ω / R21 8.2 k Ω)	Aggregate input for RK806 VCC1–12/VCCA, 3 $\times$ RK860, U8 (always-on rail)
VCC_1V1_NLDO_S3	1.1 V (derived)	U8 SY8089AAAC (L2303 2.2 μ H), EN=EXT_EN	RK806 NLDO1–5 inputs
VCC_3V3_S0	3.3 V	U3 SGM2590D (VCC_3V3_S3 $\rightarrow$ 3V3_O domain)	Upstream domain of connector 3V3_O
VCC_RTC	≈ 3 V	D2 ORing: VRTC (pin 78) $\oplus$ VCC_3V3_S3	U1 HYM8563TS RTC
HDMI_5V	≈ 4.7 V	D5 B5819WS (VCC5V0_SYSIN forward)	HDMI DDC/CEC 5 V domain (see 6.6.7)

Table 72: External Output Domains (via Connector)

Domain	Pins	Voltage	Current Capability	Remarks
3V3_O	84/86	3.3 V	TBD ($\leq$ BUCK8 3 A, additionally constrained by U3 current limit TBD)	See 6.5.1 Δ
1V8_O	88/90	1.8 V	TBD ($\leq$ PLDO2 300 mA)	See 6.5.1 Δ
VRTC	78	Provided by carrier board	—	RTC backup input (not an output)
HDMI_5V	TBD (verify against Chapter 5)	≈ 4.7 V (after D5 drop)	TBD	HDMI 5V supply output

6.6 Power-Related Control and Auxiliary Circuits

6.6.1 PMIC_ENABLE (Pin 99 $\rightarrow$ RK806 PWRON)

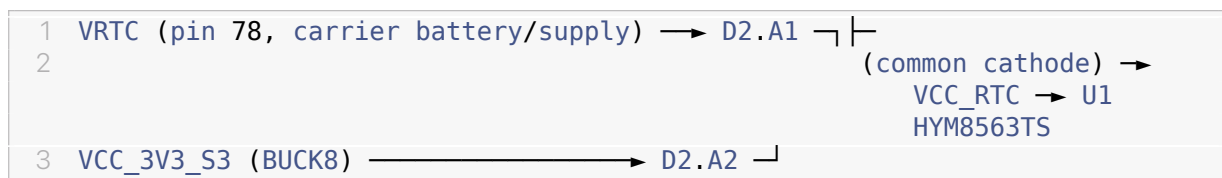
Item	Description
Signal direction	Input (to module)
Internal state	RK806 PWRON internal ~ 45 k Ω pull-up to VCCA (≈ 4 V, derived); no additional pull-up/pull-down on module
Electrical threshold	Proportional to VCCA (RK806 manual PWRON threshold definition, specific ratio TBD for verification); VDC threshold reference VIH3 = 0.88 V
Valid action	Pulled low for ≥ 20 ms: power-on (from shutdown state) / programmable debounce (500 ms); held low for 6/8/10/12 s: shutdown (0x76<6>=0) or reset (0x76<6>=1), duration programmable
Carrier-board recommendation	“Power key” connection: one end of the pushbutton to pin 99, the other end to GND; it shall not be used as a CM5-style “pull low for lowest power” level control (see 6.3.1 Δ)

6.6.2 PWR_BUT (Pin 92 → PMIC_RESET_L / RK806 RESETB Node)

Item	Description
Signal direction	Bidirectional node (reset request input / PMIC reset output)
Internal state	R2263 10 kΩ pull-up to VCC_1V8_S3 (verify power tree: pull-up source TBD for confirmation) + RK806 RESETB (open-drain in nature, TBD) + SoC NPOR (V42) + TSADC_SHUT (AC39 via R1104 0 Ω) + C2262/C1110 (0.2 μF total)
Valid action	Pulled low → SoC reset (RK806 maintains all rail outputs, see 6.3.4③)
Capacitance constraint	RK806 specifies total RESETB node capacitance to ground ≤0.3 μF ; the module already has 0.2 μF → carrier-side margin is only 0.1 μF (including reset IC output capacitance, pushbutton debounce capacitance, and cable capacitance)
Carrier-board recommendation	Connect the reset pushbutton / reset IC (open-drain) to pin 92; total additional capacitance shall not exceed 0.1 μF
Other members	SoC TSADC over-temperature (AC39, via R1104 0 Ω) actively pulls this node low to force a reset — when a low level is observed at pin 92 on the carrier board, it should be recognized that this does not necessarily originate from the pushbutton

6.6.3 VRTC and RTC Backup (Pin 78)

D2 (BAS70-05Q common-cathode dual Schottky) OR-ing:



- +5V present: VCC_3V3_S3 (3.3 V) > VRTC, D2.A2 conducts to supply the RTC;
- +5V removed: automatically switches to the carrier-board VRTC, and RTC timekeeping is maintained;
- VRTC voltage/current requirements and the impact of D2 reverse leakage on battery life are **TBD** (per U1/D2 datasheets).

6.6.4 VDC Automatic Power-on Trigger Circuit (Module-Internal)

The CM120 implements an RC-coupled automatic power-on circuit on the module (distinct from the CM5's "PMIC_EN rising-edge power-on"):

1	VCC_SYSIN	—C90408 4.7 —●—	μFD2600 B5819WS (negative clamp to GND)
2			
3		R95379 200 Ω	
4			
5	VDC pin	●—C2260 1 —nFGND; via R2265 200 Ω—	kGND

- **Principle:** upon a VCC_SYSIN step, C90408 couples a positive pulse at the VDC node with an amplitude of $\approx VCC_SYSIN \times R2265 / (R95379 + R2265) \approx 2\text{ V}$ (derived), far exceeding VDC VIH3 = 0.88 V; the decay time constant $\tau = (R95379 + R2265) \times C90408 \approx 1.9\text{ s}$, so the effective pulse width is far longer than the 2 ms power-on determination window;
- **D2600** clamps the negative-going coupled voltage (at +5V loss) to GND, protecting the VDC pin;
- **Effect:** +5V applied → the module powers on automatically (see 6.2.2①); after software shutdown, VDC returns to zero (DC blocking) and the PMIC does not power on by itself;
- On +5V re-application after a power loss: VCC_SYSIN steps again → VDC re-triggers → **automatic re-power-on**. Applications requiring "manual confirmation before power-on after power loss" shall control the +5V switching policy on the carrier-board side.

6.6.5 PMIC Management Signals

Signal	Module-Internal Connection	Remarks
PMIC_SPI (CS/CLK/...)	SoC ↔ RK806 (CS pulled down via R2258 100 kΩ to select SPI mode)	After power-on, the SoC reconfigures rail voltages/sequences (TBD firmware OTP version)
EXT_EN	RK806 → R2305 10 kΩ → U8 EN	Timing T1 = 3.5~100 ms; also master/slave selection (floating = master; single PMIC in this design, see 6.2.4)
SYNC / SYNC_CLK	Not connected externally (single PMIC)	For multi-PMIC synchronization; not used in this design
PWRCTRL	SoC (specific GPIO pin TBD for verification)	SLEEP (FUN=001) / shutdown (010) / reset (011) function selection
TSADC_SHUT	SoC TSADC → R1104 0 Ω → RESETB node	SoC over-temperature protection forced reset (see 6.6.2)

6.6.6 I2C Power Management Buses

Bus	Attached Devices	Remarks
I2C0_M2	U2300 (0x42), U2301 (0x43, addresses TBD, subject to BOM)	CPU BigCore0/1 DVFS voltage scaling
I2C2_M0	U2302 (0x42 class, address TBD) + U1 HYM8563TS (address TBD)	NPU DVFS + RTC; U2302 and U1 share the bus and their addresses shall not conflict

Both buses use 3.3 V pull-ups (**pull-up source and resistance verification: TBD**, see power tree / Chapter 5).

6.6.7 HDMI 5V (HDMI_5V)

+5V is fed unidirectionally via D5 (B5819WS Schottky) to the HDMI_5V domain (the connector HDMI 5V pin and the DDC/CEC pull-up supply). The voltage drop is ≈ 0.3 V, giving an output of ≈ 4.7 V (**TBD for measurement**). **The carrier board shall not back-feed 5 V into the module through the HDMI connector** (D5 blocks reverse current, but this shall nevertheless be avoided). Connector pin allocation per Chapter 5.

6.7 Protection Features

Summary of protection functions of the module power system (thresholds are typical values from device datasheets; CM120 system-level actions are **TBD for verification**):

Protection Item	Threshold / Condition	Device / Level	Action
+5V input undervoltage lockout UVLO	VIN < 2.4 V (typ, rising edge; 200 mV hysteresis)	U2 JW5265	VCC_SYSIN shut down (pre-regulator fails first)
Pre-regulator over-current / short circuit	PFET current limit 7.8 A (typ, 6.5 ~ 9.4 A); short circuit >1024 cycles triggers hiccup (8 ms retry)	U2 JW5265	Current limiting / hiccup protection
Pre-regulator over-temperature TSD	> 150 °C (20 °C hysteresis)	U2 JW5265	Shutdown, auto-recovery after cooling
Input undervoltage lockout UVLO	VCCA/VCC1/VCC2 < 2.7 V (typical)	RK806	Shutdown (Method ☺/SYNC☺); when 0x5F<7>=0, automatic restart after recovery
Input overvoltage lockout OVLO	VCCA/VCC1/VCC2 > 6.0 V (typical)	RK806	Same as above
System low voltage VB_LO	< 3.2 V for 1 ms (enabled when 0x5E<3>=0)	RK806	Sequenced shutdown (Method ☺)

Protection Item	Threshold / Condition	Device / Level	Action
Input validity determination VB_OK	≥ 2.8 V (typical)	RK806	Power-on precondition (6.2.1)
PMIC over-temperature TSD	> 140 °C (typical)	RK806	Sequenced shutdown (Method ⑤)
RK860 undervoltage UVLO	$V_{IN} < 2.55$ V	RK860×3	Output shutdown
RK860 overvoltage OVP	> 6 V	RK860×3	Output shutdown
RK860 over-temperature TSD	> 150 °C (typical, 25 °C hysteresis)	RK860×3	Output shutdown
RK860 over-current OCP	7 A continuous / 8.5 A peak limit	RK860×3	Current-limit protection (details TBD)
3V3_O over-current	Set by R33=4.3 kΩ, threshold TBD	U3 SGM2590D	Hiccup or latch-off (TBD)
SoC over-temperature	TSADC threshold (TBD , SoC side)	SoC TSADC → RESETB node	Forced SoC reset (6.6.2)
RESETB capacitance violation	> 0.3 μF (constraint, not a protection)	—	Carrier-board design rule (6.6.2)
+5V back-feed prevention	D5/D2 unidirectional	—	Carrier-board design rule (6.1.1/6.6.7)

Overall +5V input protection (fuse/eFuse/surge): no input protection device is populated on the module; this is the carrier board's responsibility. Carrier-board designs shall provide their own input over-current and surge protection.

7 Appendix D: Abbreviations and Definitions

Abbreviation	Definition
B2B	Board-to-Board: Refers to a connection or configuration where two circuit boards are directly connected to each other without any intermediary components or interfaces in between.
Boot Media	The storage device from which the system boots or initializes.
Bootrom	A small piece of code located in the read-only memory of a device that is responsible for the initial boot process.
Baud Rate	The number of signal changes per second in a communication channel. It represents the transmission speed of data.
CM120	Radxa CM120: The Radxa CM120 is a compact compute module developed by Radxa, featuring a powerful SoC and various integrated components for embedded computing applications.
Debug Serial Console	A communication interface used for low-level debugging and accessing system information.
eDP	Embedded DisplayPort: A display interface standard primarily used in laptops, tablets, and other embedded systems for connecting the display panel to the graphics controller.
eMMC	Embedded MultiMediaCard: A type of non-volatile flash storage commonly used in portable electronic devices, providing high-speed data access and reliable storage capabilities.
HDMI	High-Definition Multimedia Interface: A digital audio/video interface used for transmitting high-quality uncompressed audio and video signals between devices such as TVs, monitors, and projectors.
I2C	Inter-Integrated Circuit: A serial communication protocol that allows multiple devices to communicate with each other using a shared bus.
I2S	Inter-IC Sound: A serial bus interface used for transmitting digital audio data between integrated circuits, typically for connecting audio devices such as microphones, speakers, and digital audio converters.
Maskrom Mode	A mode in which the device enters when there is no bootable code found in the boot media. It allows the device to be recognized by a host PC for firmware flashing or other operations.
PCB	Printed Circuit Board: A board made of insulating material with conductive pathways etched or printed onto it to connect electronic components and provide mechanical support for circuitry.
PCIe	Peripheral Component Interconnect Express: A high-speed serial computer expansion bus standard used for connecting various peripheral devices to a computer motherboard.
PID	Product ID: A unique identifier assigned to a specific product, often used in combination with the Vendor ID (VID) to identify and differentiate devices in computer systems or networks.
SKU	Stock Keeping Unit: A unique identifier assigned to a particular product or item for inventory tracking and management purposes. It is used to distinguish between different variations or configurations of the same product.
SoC	System-on-a-Chip: An integrated circuit that integrates multiple components of a computer or electronic system, including a microprocessor, memory, input/output interfaces, and other necessary circuits, onto a single chip.
UART	Universal Asynchronous Receiver-Transmitter: A hardware component used for serial communication.
USB	Universal Serial Bus: A popular standard for connecting various peripherals and devices to a computer system.
VID	Vendor ID: A unique identifier assigned to a specific manufacturer or vendor, often used in combination with the Product ID (PID) to identify and differentiate devices in computer systems or networks.

